Doc. CS/110
21 November 2002

Candidate Standard: Synchronization Standard for Distributed Transmission

Advanced Television Systems Committee
1750 K Street, N.W.
Suite 1200
Washington, D.C. 20006
www.atsc.org

The Advanced Television Systems Committee, Inc., is an international, non-profit organization developing voluntary standards for digital television. The ATSC member organizations represent the broadcast, broadcast equipment, motion picture, consumer electronics, computer, cable, satellite, and semiconductor industries.

Specifically, ATSC is working to coordinate television standards among different communications media focusing on digital television, interactive systems, and broadband multimedia communications. ATSC is also developing digital television implementation strategies and presenting educational seminars on the ATSC standards.

ATSC was formed in 1982 by the member organizations of the Joint Committee on InterSociety Coordination (JCIC): the Electronic Industries Association (EIA), the Institute of Electrical and Electronic Engineers (IEEE), the National Association of Broadcasters (NAB), the National Cable Television Association (NCTA), and the Society of Motion Picture and Television Engineers (SMPTE). Currently, there are approximately 160 members representing the broadcast, broadcast equipment, motion picture, consumer electronics, computer, cable, satellite, and semiconductor industries.

ATSC Digital TV Standards include digital high definition television (HDTV), standard definition television (SDTV), data broadcasting, multichannel surround-sound audio, and satellite direct-to-home broadcasting.

About the Candidate Standard

This specification is being put forth as a Candidate Standard by the T3/S9 Specialist Group. This document is an editorial revision of the Working Draft (T3-587) dated 10 October 2002. All ATSC members and non-members are encouraged to review and implement this specification and return comments to dx-editor@atsc.org. ATSC Members can also send comments directly to the T3/S9 Specialist Group. The ATSC believes this specification is stable. A Candidate Standard may be updated while in review if those updates clarify existing meaning or consensus. Substantive changes that require coordination with other groups will cause the document to return to Working Draft status.

Table of Contents

Index of Tables and Figures

Candidate Standard: Synchronization Standard for Distributed Transmission

1. SCOPE

This Standard was prepared by the Advanced Television Systems Committee (ATSC) Technology Group on Distribution (T3) Specialist Group on RF Transmission (T3/S9). The document was approved by T3 on 8 October 2002 for submission by letter ballot to the membership of the Technology Group on Distribution for consideration as a Candidate Standard, as described in Section 14 of The Procedures for Technology Group and Specialists Group Operation (ATSC Doc. B/3, 21 October 2002). The document was approved by the members of T3 on 21 November 2002.

Development of the technology described herein and of this standard itself was carried out by the Merrill Weiss Group LLC.

1.1 Purpose

This document defines a Standard for synchronization of multiple transmitters emitting trellis-coded 8-VSB signals in accordance with ATSC A/53 Annex D (RF/Transmission Systems Characteristics). The emitted signals from transmitters operated according to this standard comply fully with the requirements of ATSC A/53. This document specifies mechanisms necessary to transmit synchronization signals to the several transmitters using a dedicated PID value, including the formatting of packets associated with that PID and without altering the signal format emitted from the transmitters. It also provides for adjustment of transmitter timing and other characteristics through additional information carried in the specified packet structure. The techniques defined for synchronization of multiple transmitters may also be applied to single transmitters when it is necessary or desirable to synchronize processes conducted at the input end of a transport link with those carried out at a transmitter location, as may be useful for enhanced transmission techniques.

1.2 Application

This document describes techniques that allow construction of single frequency networks (SFNs) using a multiplicity of transmitters. There are two forms of transmitter systems that can be used in SFNs: digital on-channel repeaters (DOCRs) and distributed transmission (DX) schemes. This document describes methods necessary to enable distributed transmission; DOCRs are beyond its scope, although perfectly valid for use in SFNs. Indeed, DOCRs can be used to extend and fill in the coverage from DX transmitters. The difference between the techniques is explained in Section 4.1.1.

Users of this standard are advised that, while Distributed Transmission holds the potential to greatly improve the coverage and service areas of DTV transmission, it also holds the potential to cause interference within the network that some receivers, particularly early designs, may not be able to handle. Consequently, Distributed Transmission Networks must be carefully designed to minimize the burden placed on the adaptive equalizers in such legacy receivers while maximizing the improvement in signals delivered to the public. The impact on any specific receiver will depend upon the receiver's location, the use of directional antennas, and other factors related to the design of the receiver.

The factors in network design that influence receiver performance are frequency offsets, amplitude differentials (i.e., D/U ratios), and timing differentials. Network designs may be

optimized by placing areas of interference within the network in locales having low population, through use of terrain shielding where available, by use of directional transmitting antennas, through maintenance of tight frequency control of transmitters, and by adjustment of network emission timing.

1.3 Organization

The document is organized as follows:

Section 1—Provides this general introduction.

Section 2—Lists references and applicable documents.

Section 3—Provides a definition of terms, acronyms, abbreviations, syntax formats, and code points for this document.

Section 4—Describes the terrestrial transmitter synchronization architecture.

Section 5—Specifies the transmitter cadence synchronization signals.

Section 6—Specifies the distributed transmission packet structure.

Section 7—Specifies the synchronization signal generation.

Section 8—Specifies the transmitter synchronization process.

Section 9—Specifies the transmitter mode control methods.

Section 10—Specifies the transmitter timing adjustment methods.

2. REFERENCES

The following documents are applicable to this Standard:

1) ATSC Standard A/53B (2001), ATSC Digital Television Standard (*normative*).
2) ATSC Document A/54 (1995), Guide to the ATSC Digital Television Standard (*informative*).
3) ISO/IEC 13818-1:2000, Information Technology—Generic Coding of Moving Images and Associated Audio Information: Systems.
4) SMPTE Standard for Television—Synchronous Serial Interface for MPEG-2 Digital Transport Stream, SMPTE 310M (*normative*).

3. DEFINITIONS

3.1 Compliance Notation

As used in this document, “shall” denotes a mandatory provision of this standard. “Should” denotes a provision that is recommended but not mandatory. “May” denotes a feature whose presence does not preclude compliance, and that may or may not be present at the option of the implementer.

3.2 Acronyms and Abbreviations

The following acronyms and abbreviations are used within this specification:

ATSC Advanced Television Systems Committee
bslbf bit serial, leftmost bit first
BSS buried spread spectrum (direct sequence)
CS cadence signal

DFS	data field synchronization data segment
DS	delay spread
DTV	digital television
D/U	desired-to-undesired signal ratio
DX	distributed transmission
DXA	distributed transmission adapter
DXS	distributed transmission system
DXN	distributed transmission network
DXP	distributed transmission packet
ECC	error correcting code
ERP	effective radiated power
GPS	Global Positioning System
lsb	least significant bit
Mb/s	megabits per second
MD	maximum delay
MPEG	Moving Picture Experts Group
msb	most significant bit
OD	offset delay
OMP	operations and maintenance packet
PAT	program association table
PCR	program clock reference
PID	packet identifier
PRBS	pseudo random binary sequence
riuimsbf	repeated, inverted, unsigned integer, most significant bit first
riuimsbfwp	repeated, inverted, unsigned integer, most significant bit first, with parity
SFN	single frequency network
STS	synchronization time stamp
SP	synchronization packet
RS	Reed Solomon error correcting code
TAD	transmitter and antenna delay
TS	transport stream
uimsbf	unsigned integer, most significant bit first
uipfmsbf	unsigned integer plus fraction, most significant bit first
WM	watermark
XOR	exclusive OR function

3.3 Definitions of Terms

The definitions appearing in this subsection are those that apply to terms as used in this Standard and may be different from the meanings of the respective terms in other instances.

buried spread spectrum A technique permitting carriage of data in the same spectrum with, but without interference to, another signal by transmitting that data at a much reduced level relative to the primary signal and using coding techniques to permit its recovery with adequate signal-to-noise ratio.

bury ratio The ratio, normally expressed in dB, between the average power of the primary 8-VSB signal and the power of a buried spread spectrum sharing the same channel.

data field sync The data segment added by the modulator that includes mode indicators, training signals for receiver adaptive equalizers, and similar information, and that serves as the starting point for the data processing functions that start from known states. Depending upon the context, the term can apply to Data Field Sync data segments having the middle PN-63 sequence in either phase, or it can apply only to the Data Field Sync data segments that alternate with Data Frame Sync data segments.

data frame sync The Data Field Sync data segment in which the middle PN-63 sequence is not inverted relative to the two adjacent PN-63 sequences.

data segment A part of the data framing structure, comprising 832 total symbols, that begins with a Data Segment Sync word, represented by four transmitted 2-level symbols, and carries 828 symbols of payload thereafter.

delay spread The difference in arrival times at a point in space or at a receiver input of a signal and its significant echoes or of signals emitted by different transmitters.

epoch An instant in time that is arbitrarily selected as a point of reference.

packet A collection of data sent as a unit, including a header to identify and indicate other properties of the data, and a payload comprising the data actually to be sent, either having a fixed, known length or having means to indicate either its length or its end.

RF watermark A buried spread spectrum (BSS) signal carrying codes used for the purpose of identification of the host signal with which it is associated and for carrying a small amount of low speed data.

3.4 Reserved Fields

reserved Fields in this Standard marked "reserved" shall not be assigned by the user, but shall be available for future use. Decoders are expected to disregard reserved fields for which no definitions exist that are known to that unit. Each bit in the fields marked "reserved" shall be set to one until such time as they are defined and supported.

3.5 Section and Data Structure Syntax Notation

This document contains symbolic references to syntactic elements. These references are typographically distinguished by the use of a different font (e.g., restricted), may contain the underscore character (e.g., sequence_end_code) and may consist of character strings that are not English words (e.g., dynrng).

The formats of sections and data structures in this document are described using a C-like notational method employed in ISO/IEC 13818-1. Values expressed in hexadecimal notation herein are preceded by a prefix of "0x"; thus the decimal value 123 would be denoted as "0x7B" (without the quotation marks) in hexadecimal form.

4. TERRESTRIAL TRANSMITTER SYNCHRONIZATION ARCHITECTURE (INFORMATIVE)

This section describes the concept of a single frequency network (SFN) and the types of transmission methods that can be used to construct an SFN. It explains the requirements for

transmitters and receivers to make an SFN work, and it describes the characteristics of the trellis-coded 8-VSB system (8T-VSB) that must be considered when synchronizing transmitters in the distributed transmission (DX) form of SFN. Finally, it explains the mechanisms to be used in the synchronization process.

4.1 Single Frequency Networks

Single frequency networks comprise multiple transmitters all sharing a single channel. The transmitters emit identical signals, several of which may be received more or less simultaneously by individual receivers. The receivers must treat the multiple received signals as echoes of one another, extracting the data being transmitted despite the possible interference from alternate transmitters within the SFN. The following subsections describe the workings of SFNs and the requirements for receivers and transmitters used in an SFN.

4.1.1 Multiple Transmitters Sharing a Single Channel

In order to allow receivers to treat signals arriving from multiple transmitters as echoes of one another, it is required that the transmitters emit the same signals as one another for the same data inputs. There are two basic techniques for achieving such a condition: Transmitters can repeat signals received off-the-air from other transmitters, thereby guaranteeing that they are transmitting the same signals—although with some delay—or data can be fed to each of the transmitters in parallel, with means provided to ensure that the emitted symbols from all transmitters are the same. It is the latter approach that is facilitated by this Standard.

4.1.2 Receiver Requirements

The implementation of SFNs is very much dependent upon the ability of receivers to extract data from received signals having significant levels of echoes at widely spaced time offsets. This capability includes the handling of leading echoes, or "pre-ghosts," that result from stronger signals arriving at a receiver from transmitters that are further away or have delayed emission times relative to a nearer transmitter. The time window of echoes—i.e., the "delay spread" (DS)—that can be handled by receivers partly determines how far apart transmitters can be placed in the SFN.

4.1.3 Transmitter Requirements

There are two fundamental requirements for transmitters in a single frequency network: They must emit the same output symbols for the same data inputs, and they must transmit on the same frequency. Any divergence of the output symbols from identity between transmitters will result in receivers not being able to treat the several signals as echoes of one another. Any difference in frequency will cause the apparent echoes in the signal to have the characteristics of a Doppler shift; i.e., for it to seem as though they had been reflected from moving objects. Such Doppler shifts place additional burdens on adaptive equalizers in receivers and are to be avoided.

4.1.4 Forms of Transmission Architecture

Several types of system architectures can be used for digital transmission. The classic scheme is a tall tower with a high power transmitter to cover a large area. Another fundamental approach is the use of a multiplicity of smaller towers with lower power transmitters to cover smaller areas. This is the single frequency network. Although not technically the same as a cellular communications system for a variety of reasons, the areas covered by transmitters in such a system are nonetheless often called "cells." SFNs can be designed using a few cells covering

relatively large areas—the so-called "large cell" scheme—or they can be designed with many cells covering relatively small areas—the "small cell" scheme.

4.2 Distributed Transmission Concept (Transmitter Diversity)

Distributed transmission, or *transmitter diversity*, is unlike any method used in broadcasting in the past. Previously, translators and boosters (on-channel translators) have been used to extend the service areas or fill in gaps in coverage of conventional, high power broadcast stations. Such techniques have been applied to both FM radio and television broadcasting. The power levels of the translators and boosters are generally low, and the service they provide is treated as secondary in class.

Distributed transmission (DX) is intended to use a multiplicity of transmitters to cover a service area without necessarily requiring inclusion of a conventional, high power station, although one or more may be part of the network of transmitters. DX allows the signal levels throughout a service area to be higher than they would be from a single transmitter, and it also permits better control of interference to neighboring stations. The techniques for achieving these advantages are well understood but beyond the scope of this Standard.

The remainder of this subsection will examine some of the system considerations in the use of DX techniques. This examination will provide necessary background information for the specifications in the later portions of this Standard.

4.2.1 Difference from On-Channel Repeaters

On-channel repeaters have been used for some time in the FM radio and the television services to fill in gaps in coverage and occasionally to extend service areas. On-channel repeaters fundamentally receive signals over the air from the main transmitter, from other on-channel repeaters, or from translators and retransmit those signals on the same channel. Because they are essentially amplifiers connected between a receiving and a transmitting antenna, care must be taken in the design of on-channel repeaters to avoid the signal distortions caused by feedback around the amplifier or, worse, oscillation. As a consequence of the need to avoid feedback, on-channel repeaters are limited in power to a few tens or perhaps hundreds of watts effective radiated power (ERP). Distributed transmission has no such power limitations and does not suffer from signal degradation due to feedback.

4.2.2 Direct Feed to Each Transmitter

Implicit in distributed transmission is the use of a direct feed to each transmitter. This allows power levels sufficient for large cell designs that would be impossible with on-channel repeaters. The signals fed to the transmitters can be fully modulated and carried on analog distribution media, requiring only up-conversion to the output channel and amplification, or they can be digital signals requiring data processing and modulation at each transmitter. The use of digital signal distribution results in cleaner emitted signals and may require less bandwidth on the distribution system.

4.2.3 Multiplicity of Delivery Methods

There is a multiplicity of methods for delivering the signals from the studio source to the several transmitters in a distributed transmission system. Discounting analog delivery because of the noise added to the delivered signal, digital circuits can include fiber optics using a variety of protocols, satellite data delivery, and microwave transmission. In each case, it is desirable to keep the data rate to the minimum necessary to deliver the packets to be transmitted. The method

described in this Standard maintains the data rate of the transport streams delivered to the transmitters at the same rate as used for the payload in the transmission process, which is the same rate used in conventional 8-VSB transmission (19.39 Mb/s).

4.2.4 Transmission of Identical Symbols

In a single frequency network, it is imperative that the symbols emitted by each of the several transmitters be identical for identical data inputs. The 8-VSB transmission standard embodied in ATSC A/53 makes provision for the synchronization of certain parts of the data processing that takes place before modulation, but it does not relate that synchronization to specific points in the input data stream. Thus, while the relationship between portions of the data processing system is specified, the relationship between those elements and the input data will be random, depending upon when the modulator is switched on. Moreover, there are processes within the 8-VSB standard that are stochastic and have no fixed relationship at all to the input data stream. Consequently, without further specifications, the requirement for transmission of identical symbols for identical inputs cannot be met by the existing 8-VSB standard. It is the purpose of this Standard to provide the necessary synchronization specifications.

4.2.5 Delay Spread Control

When identical symbols are transmitted from multiple transmitters, receivers will experience those signals as one or more primary signals and echoes dispersed in time. The total time between the soonest arriving signal and the latest arriving signal is called the *delay spread*. When the desired-to-undesired (D/U) signal ratio between transmitters in a network falls below a certain value, the delay spread capability in receivers becomes significant in determining whether data can be reliably recovered from the several signals that may be present at a given receiver's location. This factor becomes more significant as the size of cells grows larger. To minimize the delay spread capability required in receivers, control of the time of emission of the signals from transmitters in the network can be used to adjust the delay spread over the service area. Thus, an important element of the synchronization system for distributed transmission is the ability to control the relative emission time of the transmitters in the network.

4.3 Elements of 8T-VSB Transmission

An 8T-VSB modulator consists of two basic sections: one for data processing and one for signal processing. To achieve the synchronization necessary in SFNs between the output symbols of transmitters that receive separate data feeds as inputs, it is necessary to synchronize the various data processing blocks. This subsection examines each of those blocks in processing order, as defined in ATSC A/53 Annex D, with particular reference to the timing of the operations performed by the respective blocks.

4.3.1 Data Randomization

The data randomizer exclusive-ORs (XORs) all the incoming data bytes with a 16-bit maximum length pseudo random binary sequence (PRBS) that is initialized at the beginning of each Data Field. Data Fields always begin at the start of an MPEG-2 Transport Stream (TS) packet. In unsynchronized 8T-VSB, the modulator randomly selects the packet that begins a Data Field. To achieve synchronization between transmitters, the first packet in a Data Field must be identified so that all transmitters in a network initialize their PRBS values on the same TS packet.

4.3.2 Reed Solomon ECC

The Reed Solomon (RS) error correcting code is applied individually to each packet in the transport stream. Packets are processed synchronously with data segments in each Data Field. Since there is a defined phase relationship between data segments and Data Fields, there is no need for any special synchronization of the RS coding processes between transmitters in a network; they will be inherently synchronous so long as the Data Fields are synchronized.

4.3.3 Byte Interleaving

The byte interleaver employed in the 8T-VSB transmission system is a 52 data segment (intersegment) convolutional byte interleaver. Only data bytes are interleaved. Since there are 312 active data segments in a Data Field, interleaving recurs exactly 6 times during a Data Field. The interleaver is synchronized to the first data byte of the Data Field. To achieve synchronization between transmitters, all transmitters in a network must initialize their byte interleavers to the first data byte in a Data Field. The Distributed Transmission system provides a means of identifying this first data byte.

4.3.4 Bit Interleaving

Intrasegment (bit) interleaving is also performed for the benefit of the trellis coding process. The bit interleaver works in conjunction with a series of 12 pre-coders and trellis coders to convert data bytes to pre-coded and trellis-coded symbols. The conversion starts with the first data segment of the Data Field and proceeds with groups of 4 data segments until the end of the Data Field. 312 active segments per Data Field divided by 4 yields 78 conversion operations per Data Field. To achieve synchronization between transmitters, all transmitters in a network must initialize their bit interleavers on the first data byte in a data field, in the same way that the byte interleavers are synchronized.

4.3.5 Pre-Coding

The pre-coder is used to compensate for comb filters used in receivers for reduction of co-channel interference from NTSC signals. It has one bit of memory that carries across data segment and data field boundaries. The state of the memory at any given instant is dependent on the data that came prior to that time, with no initialization done at any time. Thus, the pre-coder cannot be synchronized by identification of any element of the data signal fed to the transmitter. The method for dealing with this characteristic of the pre-coding process is described in Section 6.3.

4.3.6 Trellis Coding

The trellis coder is used to extend the reception threshold of the receiver by permitting use of soft-decision decoding. It has two bits of memory that carry across data segment and data field boundaries. The state of the memory at any given instant is dependent on the data that came prior to that time, with no initialization done at any time. Thus, the trellis coder cannot be synchronized by identification of any element of the data signal fed to the transmitter. The method for dealing with this characteristic of the trellis coding process is described in Section 6.3.

4.4 Synchronization Requirements

The characteristics of the various data processing blocks of the modulator lead to a set of requirements for synchronizing those functions in a group of separately located transmitters.

Requirements exist with respect to frequency synchronization, data frame synchronization, and pre-coder/trellis coder synchronization.

4.4.1 Frequency Synchronization

If the signals arriving at a receiver from multiple transmitters are to be treated as echoes of one another, the frequencies of those transmitters must be close enough to one another that the receiver is not over-burdened with apparent Doppler shift between the signals. This requires that the output frequencies of the transmitters be tightly controlled and maintained with respect to one another.

4.4.2 Data Frame Synchronization

As demonstrated in Section 4.3, the data randomizers, Reed Solomon error correction coders, byte interleavers, and bit interleavers of 8T-VSB modulators can be synchronized with one another by properly identifying a starting point for the Data Field, since they all synchronize to it. One more element must be synchronized, however; that is the Data Field Synchronization (DFS) segment that is inserted by the modulator. The DFS carries several PRBS sequences used as training signals for adaptive equalizers in receivers. One of those PRBS sequences alternates in phase from DFS-to-DFS. This creates a Data Frame structure composed of two Data Fields. Because of the integer phase relationship between the Data Frame and its two Data Fields, it is possible to synchronize the Data Frame structure and derive the Data Fields from the Data Frame structure.

4.4.3 Pre-Coding/Trellis Coding Synchronization

As demonstrated in Section 4.3, the pre-coder and trellis coder are stochastic processes not susceptible to initialization by a regularly recurring event in the data stream. Thus, if they are to be synchronized in multiple transmitters, it is necessary to develop a state condition for the pre-coder and trellis coder memories to be applied at a specific epoch in the data stream simultaneously by all transmitters in a network. This is the method adopted by this Standard.

4.5 Synchronization Mechanisms

The synchronization requirements outlined in Section 4.4 lead to the reference top-level system configuration shown in Figure 4.1. The system comprises three elements: an external time and frequency reference (shown as GPS), a Distributed Transmission Adapter (DXA) situated at the source end of the distribution (studio-to-transmitter link, STL) subsystem, and a slave synchronization subsystem included in each of the transmitters. The heavy lines in Figure 4.1 show the paths taken by synchronization signals generated in the DXA, and a bar across the top of the figure shows the area of applicability of this standard.

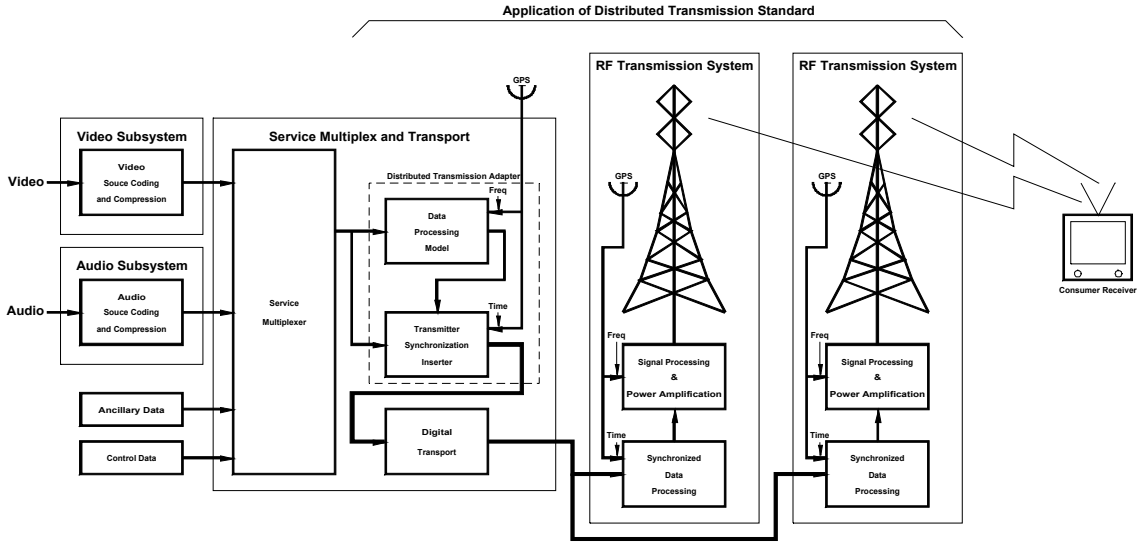


Figure 4.1 Synchronized DTV transmitter block diagram.

4.5.1 Distributed Transmission Adapter at Source

The Distributed Transmission Adapter (DXA) is used to create a pair of synchronization signals that are multiplexed into the Transport Stream prior to distribution over the STL system. The signals produced by the Distributed Transmission Adapter are a Cadence Signal (CS), which establishes the phase of the Data Frames relative to the TS packets, and a Distributed Transmission Packet (DXP), which carries information for slaving the pre-coders and trellis coders in the transmitters, indicates operating mode to the transmitters, and carries command information specifying the necessary time offset for each transmitter. To accomplish these functions, the Distributed Transmission Adapter includes a Data Processing Model equivalent to the data processing subsection of an A/53 modulator to serve as a master reference to which the slave synchronizers at the transmitters are slaved.

4.5.2 Slave Synchronization of Transmitters

At each transmitter, a Slave Synchronizer is employed to capture the Cadence Signal and the Distributed Transmission Packet, to slave the Data Frame phasing to the Cadence Signal, and to slave the pre-coder and trellis encoder to the data in the Distributed Transmission Packet (DXP). The Slave Synchronizer extracts mode information from the DXP to set the transmitter to the desired mode. It also extracts time offset command information addressed to its associated transmitter and uses it to adjust the emission time of the output symbols (as explained in Section 6.5).

4.5.3 External Time and Frequency Reference

A common time and frequency reference (such as GPS) is required at several locations in the system. The time component of the external reference is used by the Distributed Transmission Adapter to produce the time-offset information to be sent to the Slave Synchronizers to adjust the emission times of their associated transmitters. The DXA uses the frequency component to precisely maintain its output Transport Stream data rate to tight tolerances. The time component also is used by the Slave Synchronizers at the transmitters to adjust the emission times of the

associated signals to the time offsets sent from the Distributed Transmission Adapter. The frequency component also is used by the Slave Synchronizers at the transmitters to precisely set the frequencies of the transmitters in order to minimize the apparent creation of Doppler shift and the consequent burdening of receiver adaptive equalizers by frequency differences between transmitters.

5. SYNCHRONIZATION CADENCE SIGNALS (NORMATIVE)

Synchronization of the Data Frame Segment insertion and of the data processing functions that are synchronous with the Data Field structure shall be accomplished by sending a Cadence Signal from the distribution system source to each transmitter as described in this section.

5.1 Periodic Sync Word Inversion

The Cadence Signal is a periodic inversion of the MPEG-2 Transport Stream packet sync word.

5.1.1 Every 624 T/S Packets

The Cadence Signal shall be inserted regularly, once every 624 packets, in the MPEG-2 Transport Stream that shall be sent from the Distributed Transmission Adapter to each of the transmitters. Its appearance in the Transport Stream shall be associated with the payload of whatever packet occurs at the time at which a CS is required to be sent. Its appearance in the Transport Stream transported to the transmitters shall cause the output from the transmitters of the Data Field Sync data segment having no inversion of the middle PN-63 sequence. (For purposes of this document, this shall be called the Data Frame Sync data segment.)

5.1.2 0x47 Normal Sync Word

The normal MPEG-2 packet sync word is 0x47. It shall be replaced with the inverted value specified in Section 5.1.3 at the periodicity specified in Section 5.1.1.

5.1.3 0xB8 Cadence Sync Word

The Cadence Signal shall constitute the bit-wise inverse of the normal MPEG-2 Transport Stream packet sync value. Therefore, it has a value of 0xB8.

6. DISTRIBUTED TRANSMISSION PACKET STRUCTURE (NORMATIVE)

Synchronization of the pre-coder and trellis coder functions of the data processing blocks, which are not synchronous with the Data Field or any other defined structure, shall be accomplished by the sending of Distributed Transmission Packets (DXPs) as described in this section from the Distributed Transmission Adapter (DXA) to each transmitter. DXPs are a specific form of Operations and Maintenance (O&M) Packet, as explained in Section 6.1.

A DXP passes through three stages of formatting as it moves from the service multiplexer, through the DXA to the transmitters, and then through the transmitters. In each stage, the DXP has a different set of semantics. It is formatted with a fixed set of payload values when it is first formed in the service multiplexer. The formatting of the payload upon formation in the service multiplexer is described in Section 7.2.2, Distributed Transmission Packet Pre-Processing Payload. The initial payload is replaced in two stages in the DXA as described in Section 7.4, Distributed Transmission Packet Payload Substitution, to form a packet having the semantics described in this Section 6 for distribution to the transmitters. At the transmitters, part of the DXP payload is restored to its initial values, as described in Section 8.3, Distributed Transmission Packet Payload Replacement.

6.1 Operations and Maintenance Packet Structure

The Operations and Maintenance Packet (OMP) structure can be used to support a variety of operations and maintenance functions in a system. It can have various data structures, depending upon the purposes it serves in specific applications. The first such packet structure defined is the Distributed Transmission Packet.

6.1.1 Transport Header Constraints

The header of an Operations and Maintenance Packet shall conform to the structure specified for MPEG-2 Transport Stream packets in ISO 13818-1 Systems, which defines a 4-byte header and a 184 byte payload. The header and payload contents are as defined in the following sections.

6.1.1.1 PID Assignment and OM Type

The header contains a 13-bit Packet Identifier (PID) field. One value is defined to identify an Operations and Maintenance packet. The assigned PID value shall be 0x1FFA. This Standard defines use of the OMP to identify Distributed Transmission Packets.

6.1.1.2 Bit States

The remaining bits in the Operations and Maintenance Packet header shall be set as follows (binary notation): Transport Error Indicator = 0; Payload Unit Start Indicator = 1 (not used); Transport Priority = 1 (not used); Transport Scrambling Control = 00 (not scrambled); Adaptation Field Control = 01 (payload only); Continuity Counter = 0000 to 1111, incremented by one on each occurrence of the DXP and recycling from 1111 to 0000.

6.1.2 Operation and Maintenance Packet Payload Structure

In an OMP, the first byte of the 184-byte payload indicates the type of data structure contained in the remainder of the payload. The syntax of the OMP 184 byte payload shall be as shown in Table 6.1, and the semantics shall be as described in the paragraphs that immediately follow it.

Table 6.1 Operations and Maintenance Packet (OMP) Organization

Syntax	Bits	Format
OM_packet () {		
OM_type	8	bslbf
OM_payload	8*N	bslbf
}		

OM_type This 8-bit field shall be set to a value of 0x00 to indicate a Distributed Transmission Packet. All other values of OM_type are reserved by ATSC and may be used in other standards. The ATSC Code Points Registry will contain a reference to any such definition.

OM_payload This field comprises the 183 bytes in an OMP following the standard MPEG-2 Transport Stream header and the OM_type field. For OM_type 0x00, this field shall be the DX_packet () as defined in Table 6.2.

6.2 Distributed Transmission Packets

Distributed Transmission Packets shall constitute a particular form of Operations and Maintenance Packet as identified by their OM_type value. Distributed Transmission Packets shall comprise a header, trellis coder state data, transmitter mode control data, transmitter timing

control data, and Reed-Solomon error correction coding, as well as several additional items of information. The structure of a Distributed Transmission Packet shall be as shown in Table 6.2 and in the following text, which express the same information in the pseudo-C language format used by the MPEG-2 standards. The overall structure of a Distributed Transmission Packet is shown in Figure 6.1.

Table 6.2 Distributed Transmission Packet (DXP) Organization

Syntax	Bits	Format
DX_packet () {		
reserved	8	0xFF
for (i=0; i<12; i++) {		
trellis_code_state	8	riuimsbfwp
}		
transmitter_mode_control	48	riuimsbf
dfs_reserved	184	riuimsbf
reserved	8	0xFF
synchronization_time_stamp	24	uimsbf
maximum_delay	24	uimsbf
reserved	72	0xFF FFFF FFFF FFFF FFFF
tx_group_number	8	uimsbf
for (i=0; i<16; i++) {		
tx_address	12	uimsbf
tx_identifier_level	3	uimsbf
tx_data_inhibit	1	bslbf
tx_time_offset	16	tcimsbf
tx_power	12	uipfmsbf
reserved	4	'1111'
}		
tx_identifier_address	12	uimsbf
reserved	4	'1111'
tx_identifier_pattern	12	uimsbf
reserved	4	'1111'
network_identifier_pattern	12	uimsbf
reserved	20	0xFFFFF
reed-solomon_error_correcting_code	160	uimsbf
}		

trellis_code_state An 8-bit field carrying two copies of the three bits of the state of a precoder and trellis encoder pair plus parity, with one copy bit-inverted from the other.

transmitter_mode_control This 48-bit field carries 24 bits of data that indicate the mode setting of the transmitters. The 24 bits are divided into groups of four, each of which is carried in two copies within one of the six bytes of the field, with one copy bit-inverted from the other.

dfs_reserved This 184-bit field carries 92 bits of reserved data to be inserted into the Data Field Sync data segment. The 24 bits are divided into groups of four, each of which is carried in two copies within one of the 23 bytes of the field, with one copy bit-inverted from the other.

synchronization_time_stamp A 24-bit unsigned integer field that indicates the elapsed time, measured in 100 ns increments, between a 1-second tick of the reference clock and the release from the DXA of the first bit of the first Cadence Sync word following the DXP in which the field is contained.

maximum_delay A 24-bit unsigned integer field that indicates the time delay setting in the system, measured in 100 ns increments, between the output time of the DXA and the time of emission of the corresponding symbol from each of the transmitters.

tx_group_number An 8-bit unsigned integer field that carries the first 8 bits of the 12-bit addresses of the group of transmitters to which information is individually addressed in the packet instance. This field provides redundant information to improve reliability of the addressing of data to the transmitters.

tx_address A 12-bit unsigned integer field that carries the address of the transmitter to which the following fields are relevant.

tx_identifier_level A 3-bit unsigned integer field that indicates to which of 8 levels (including off) the RF watermark signal of each transmitter shall be set.

tx_data_inhibit A 1-bit field that indicates when the tx_data information should not be encoded into the RF watermark signal.

tx_time_offset A 16-bit signed integer field that indicates the time offset, measured in 100 ns increments, from the reference time determined using maximum_delay and the time of emission of the individual transmitter to which it is addressed.

tx_power A 12-bit unsigned integer plus fraction that indicates the power level to which the transmitter to which it is addressed should be set. The most significant 8 bits indicate the power in integer dB relative to 0 dBm, and the least significant 4 bits indicate the power in fractions of a dB.

tx_identifier_address A 12-bit unsigned integer field that specifies the transmitter to which the following identifier pattern data is addressed.

tx_identifier_pattern A 12-bit unsigned integer field representing the specific transmitter that provides the seed value for 12 of the 24 bits used to set the symbol sequence of a unique code assigned to each transmitter.

network_identifier_pattern A 12-bit unsigned integer field representing the network in which the transmitter is located that provides the seed value for 12 of the 24 bits used to set the symbol sequence of a unique code assigned to each transmitter.

reed-solomon_error_correcting_code A 160-bit unsigned integer field that carries 20 bytes worth of error correcting code used to protect the remaining 164 payload bytes of the packet.

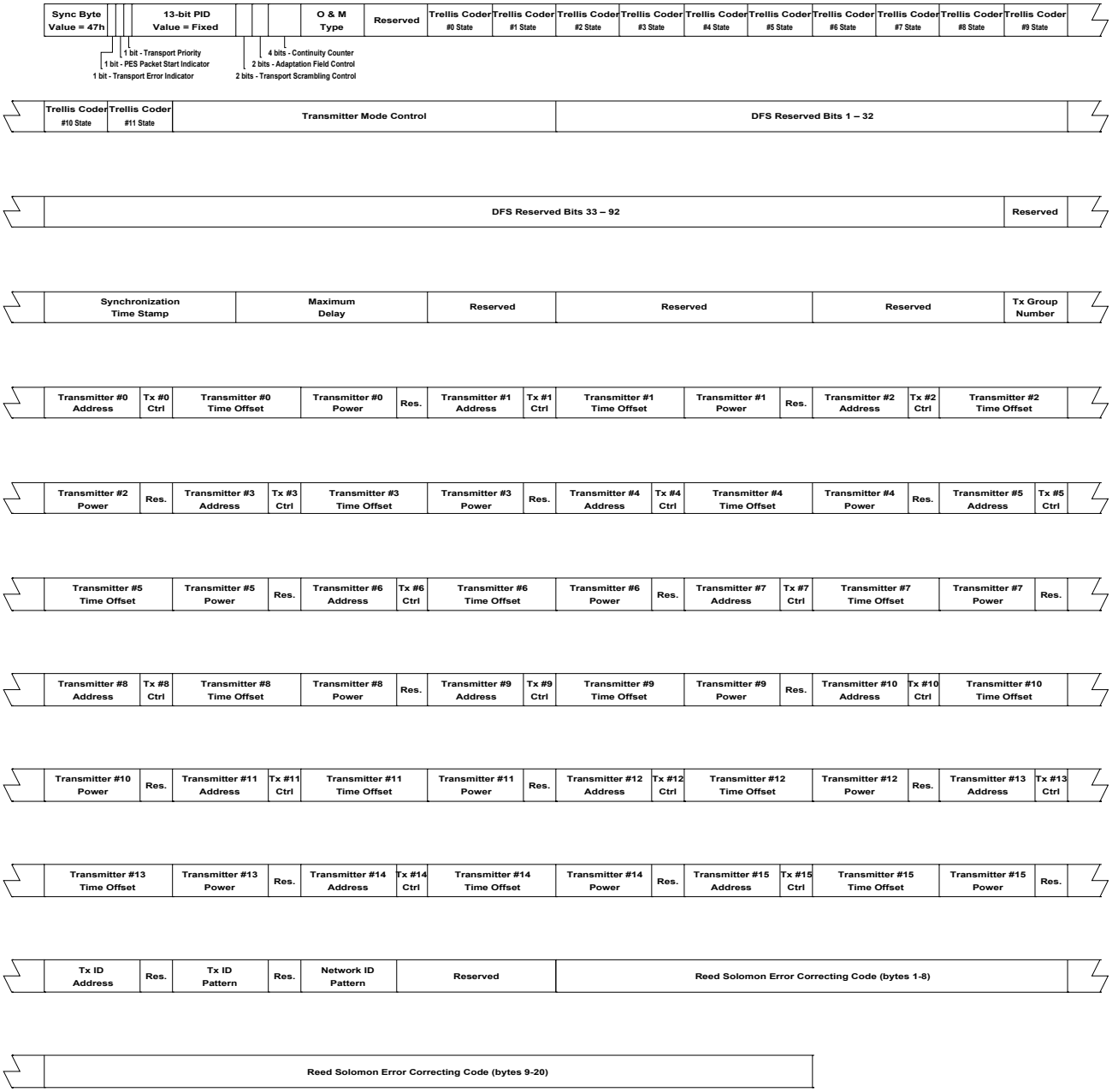


Figure 6.1 Distributed transmission packet layout.

6.3 Trellis Code State Data

Trellis Code State Data shall comprise a total of 36 bits, drawn in 3-bit groups from each of the 12 independent pre-coder and trellis encoder combinations making up the overall pre-coder and trellis encoder system inside the symbol interleaver. The extraction of the bits from the data processing model at the Distributed Transmission Adapter shall be carried out according to the methods illustrated in Figure 6.2, which shows the trellis coder synchronization source, and

Figure 6.3, which shows the trellis code interleaver synchronization source. (Note that the designations of signals in Figure 6.2 match those of A/53, Annex C, Figure 7.8.)

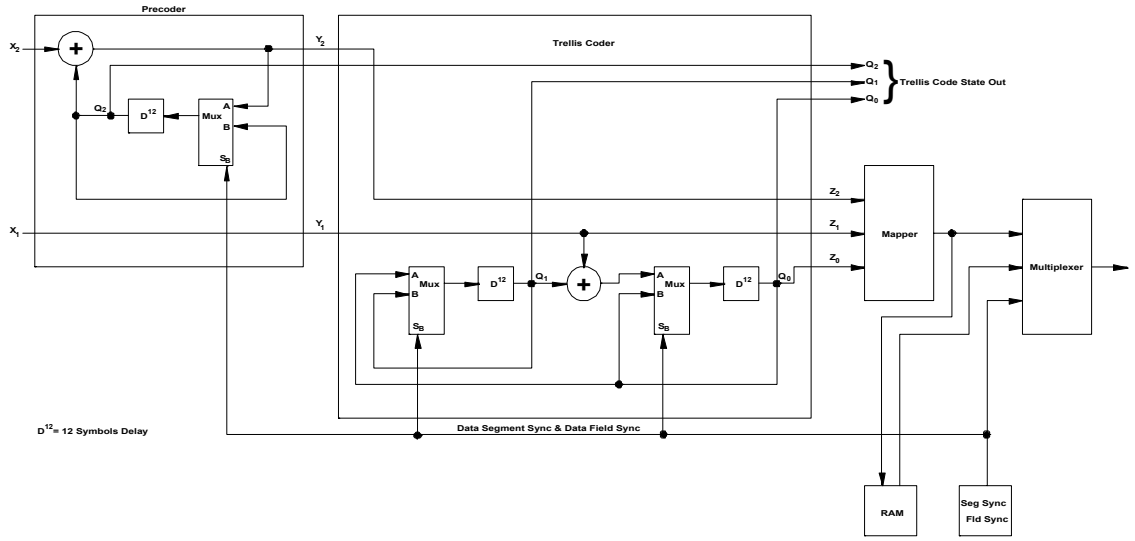


Figure 6.2 Trellis coder synchronization source.

6.3.1 State of Trellis at Next Data Frame Start

The Trellis Coder State Data shall represent the states of the 36 storage devices in the pre-coder and trellis coder subsystem of the data processing model of the Distributed Transmission Adapter, as they will be immediately following Data Field Sync at the start of the next Data Field following the appearance of the DXP in the MPEG-2 Transport Stream.

6.3.2 Format

The Trellis Coder State Data shall be packaged into the first twelve payload bytes (the trellis_code_state fields) following the OM_type and reserved fields, each byte carrying the three bits of state data derived from the corresponding one of the twelve pre-coder and trellis coder combinations conceptually used in the system; i.e., the first payload byte shall carry the data from pre-coder and trellis coder 0, the second payload byte shall carry the data from pre-coder and trellis coder 1, and so on. The twelfth payload byte shall carry the data from pre-coder and trellis coder 11.

A parity bit (even) shall be added to the three data bits from each combination of pre-coder and trellis coder, and the resulting four bits also shall be carried inverted bit-by-bit in the same byte for redundancy. Specifically, the three non-inverted bits of trellis coder state data plus parity shall be carried in the most significant bits (bits 4–7) of the byte corresponding to the particular pre-coder and trellis coder combination. The bits shall be ordered so that Z_0, Z_1, and Z_2 of Figure 6.2 are placed in bits 4, 5, and 6, respectively, of the corresponding byte. The msb (bit 7) shall carry the even parity bit for the next three lower bits. The four lsb's of the byte (bits 0–3) shall carry the inverses of the corresponding bits, four bits higher in rank in the same byte (i.e., $b0 = \overline{b4}$, $b1 = \overline{b5}$, $b2 = \overline{b6}$, and $b3 = \overline{b7}$). The structure of a Trellis Coder State byte is shown in Figure 6.4.

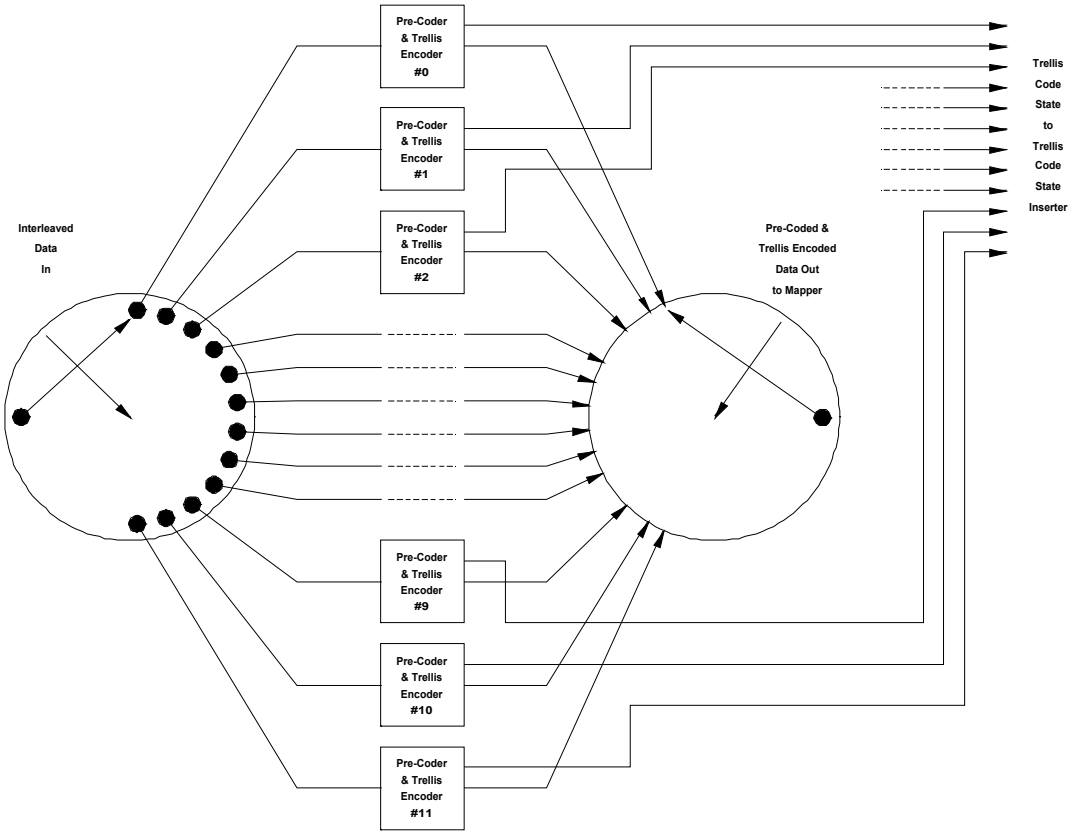


Figure 6.3 Trellis code interleaver synchronization source.

6.4 Transmitter Mode Control Data

The ATSC Digital Television Standard A/53 provides 24 bits in the Data Field Sync data segment to indicate the VSB Mode that is transmitted. It also provides an additional 92 bits immediately following the VSB Mode bits that are reserved for future use. Those bits can be used not only to inform receivers of the mode being transmitted but also to control the mode of operation adopted by the transmitters in a system. It is beyond the scope of this document to define the uses of the VSB Mode and Reserved bits, but the transmission of their values to transmitters for purposes of control is defined.

6.4.1 Addressed to All Transmitters

The group of 29 payload bytes immediately following the Trellis Coder State Data shall be used to carry VSB Mode and other control information, 4 bits per byte, to all transmitters in a network. The Transmitter Mode Control Data shall be used to set the VSB Mode of each transmitter and to provide other control functions that must be followed by all transmitters in unison. When changes occur in the Transmitter Mode Control Data, they shall become effective in the operating mode of all transmitters in the network at the end of the first complete data field following delivery of the changed data to the transmitters. In other words, the second Data Field Sync data segment following delivery of the changed data to the transmitters shall be the first data segment to adopt the new mode of operation.

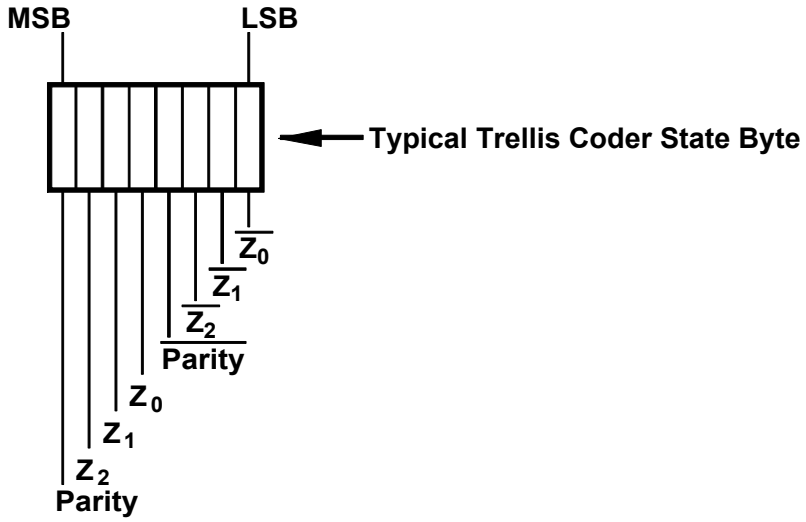


Figure 6.4 Trellis coder state byte layout.

6.4.2 Bits for Data Field Sync Transmission

The transmitter_mode_control and the dfs_reserved bits shall be transmitted by the transmitters in a network in the Data Field Sync data segment in the locations of the VSB Mode and the Reserved bits. Any changes occurring in the transmitter_mode_control and the dfs_reserved bits shall be transmitted in the first Data Field Sync data segment following delivery of the changed data to the transmitters. This timing provides a delay of one data field period between initial transmission of the changed transmitter_mode_control and/or dfs_reserved bits and the time at which the transmitters actually adopt any new mode in order to provide time for receivers to prepare for the mode change.

6.4.3 Format

The Transmitter Mode Control Data shall be divided into 29 groups of four bits each, starting with the first of the 24 VSB Mode bits to be transmitted and ending with the last of the 92 Reserved bits to be transmitted. Each group of four bits shall be carried in the msb's of one byte. In each byte, the first bit to be transmitted shall be carried in bit 7, the second in bit 6, the third in bit 5, and the fourth in bit 4. The four lsb's of the byte (bits 0–3) shall carry the inverses of the corresponding bits, four bits higher in rank in the same byte (i.e., $b0 = \overline{b4}$, $b1 = \overline{b5}$, $b2 = \overline{b6}$, and $b3 = \overline{b7}$). The structure of a Transmitter Mode Control Data byte is shown in Figure 6.5.

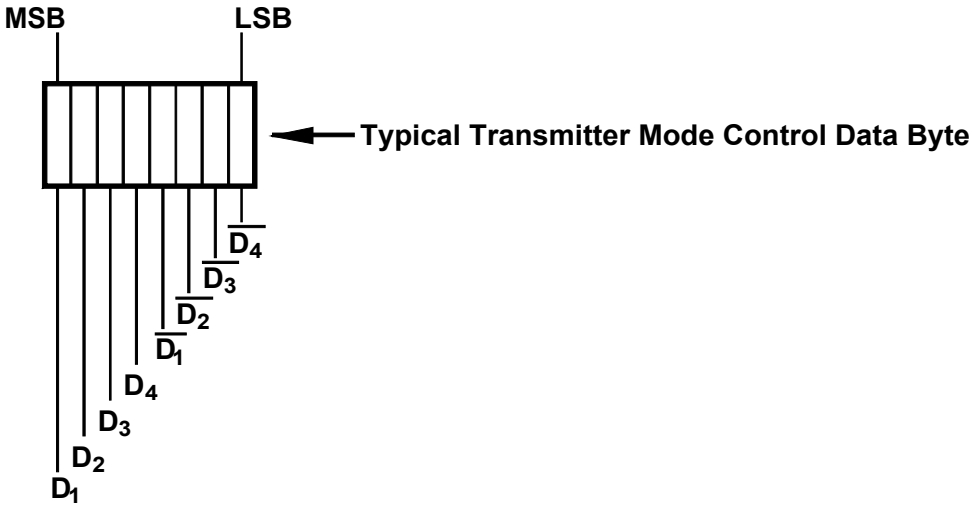


Figure 6.5 Transmitter mode control data byte layout.

6.5 Transmitter Timing Control Data

In order to enable multiple transmitters in a single frequency network to be set to transmit their signals in specific time relationships to one another, it is necessary to provide a time reference to all transmitters and to offset some or all of them in time by amounts determined by the network design. While such timing adjustments could be made on a fixed basis, in far-flung networks, it can be quite helpful to have means to adjust the timing of transmission remotely. Thus, provision is made in the Distributed Transmission Packet to carry timing control information individually to each of the transmitters in a network.

The transmitter timing control function operates by sending two time reference values to all transmitters and a third time value to each transmitter individually. The two time reference values sent to all transmitters are a Synchronization Time Stamp (STS) and a Maximum Delay (MD) value. The third time value is an Offset Delay (OD) that is specific to each transmitter. The emission time for each transmitter is the combination of STS, MD, and OD. The timing is dependent upon a common time reference (such as GPS time) being available to each of the nodes in the network, including the Distributed Transmission Adapter and each of the transmitters. The relationships between the various elements of the transmitter timing control data are shown in Figure 6.6.

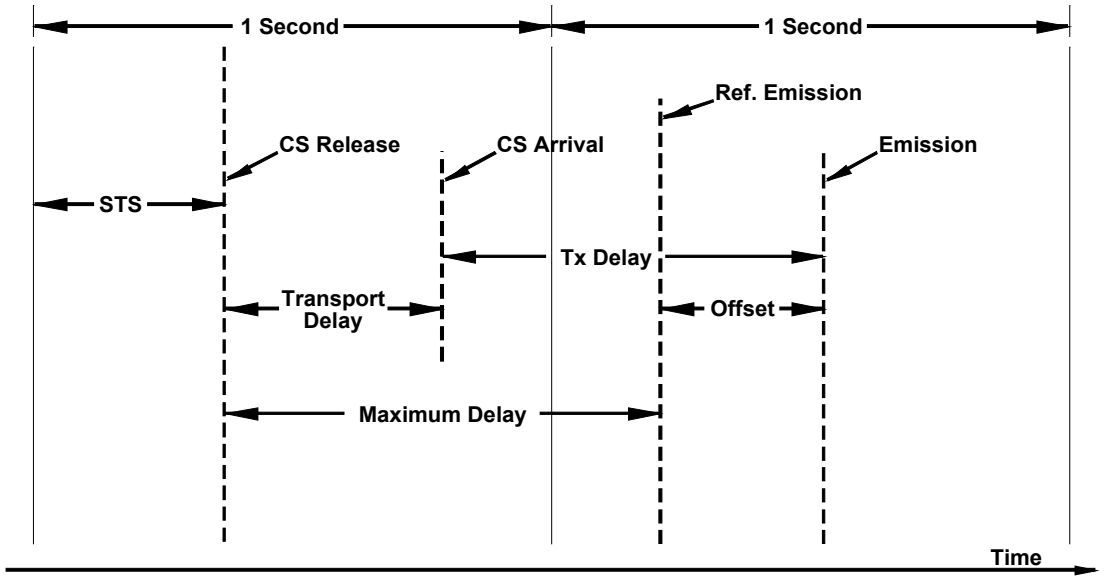


Figure 6.6 Transmitter timing control relationships.

6.5.1 Synchronization Time Stamp (STS)

The Synchronization Time Stamp (STS) shall be the number of 100 ns time intervals between the last 1 second clock tick of the common time reference and the start of the next data frame following the Distributed Transmission Packet, as determined by the start of the next Cadence Sync word at the output of the Distributed Transmission Adapter (see Section 7).

6.5.2 Maximum Delay (MD)

The Maximum Delay (MD) shall be a value that is set as a system parameter so as to assure that the output times of all transmitters in the network will be delayed sufficiently to account for the longest delay in the distribution path to any transmitter plus the delay of the transmitter itself and its antenna system. It shall be measured in 100 ns time intervals and shall take a value between a lower and an upper bound such that, when MD is added to the Offset Delay (OD) plus the delay time of the transmitter and antenna system, the total neither falls below 0x000001 nor exceeds 0x98967F (i.e., the total falls within the range between one count and one count less than 1 second). Nominal lower and upper bound values of MD of 0x008064 and 0x98161C, respectively, can be considered usable without further calculations. In unusual situations in which it is necessary to more closely approach the limiting values, care should be used to calculate the total of all delays so that the limits of one count more than zero and of one count less than one second are not exceeded under any circumstances of system operation. The values given are sufficient to allow for distribution systems using satellite transponders to reach transmitters in a network.

6.5.3 Offset Delay (OD)

The Offset Delay shall be a value that is set as a parameter for each transmitter so as to allow adjustment of the emission timing of transmitters with respect to one another. It shall be measured in 100 ns time intervals and shall take a value between –32,768 and 32,767 (i.e., from

–3.2768 ms to 3.2767 ms). The OD for each transmitter shall be compensated for the Transmitter and Antenna Delay (TAD) of that transmitter, which value shall include the total delay from the system point at which the transmitter output timing is measured and controlled to the output of the antenna. The TAD compensation shall be performed through a calculation carried out by the transmitter using a fixed value of TAD determined for that transmitter. The total spread between emission times of transmitters in a network thus can be up to 6.5535 ms (possibly limited by any differences in transmitter and antenna system delays).

6.5.4 Emission Time for Next Data Frame Start

The reference time for the start of transmission of the first Data Segment Sync following the first Data Frame Sync data segment following the Distributed Transmission Packet shall be the Synchronization Time Stamp value plus the Maximum Delay value (STS + MD). Each transmitter in a network shall use that reference time plus the Offset Delay (OD) for that transmitter, compensated by that transmitter's TAD value, to determine its emission time for the leading edge (zero crossing of the +5 to –5 transition) of the first Data Segment Sync following the first Data Frame Sync data segment following arrival of the Distributed Transmission Packet.

6.5.5 Determining Emission Delay

A transmitter may determine the delay required (Tx Delay in Figure 6.6) between its reception from the transport system of any given Cadence Sync word and emission of the corresponding first Data Segment Sync following the Data Frame Sync data segment by measuring, in 100 ns time intervals, the time from the last 1 second tick of the common time reference to the time at which it receives the Cadence Sync word first following a Distributed Transmission Packet (CS Arrival). That value subtracted from the emission time for that transmitter equals the delay time required, in 100 ns time intervals.

6.6 Transmitter Identification and Signaling

In a distributed transmission network, identifying each of the transmitters when it is received over the air can be a difficult proposition. This difficulty occurs because the signal from each of the transmitters is intentionally made to be identical to all the others so that adaptive equalizers in receivers can treat them as echoes of one another. Yet it can be very useful to determine which transmitters are being received at a particular location and, indeed, what their contributions are to the aggregate received signal in order to permit optimization of the network adjustments. (It can also be very useful to identify interfering transmitters from another DX Network or a conventional digital transmitter.) So as to allow identification of individual transmitters, provision is made to assign specific, identifiable codes to particular transmitters, the assignment of which is communicated through the DXP. Moreover, a similar code to identify the network is also communicated through the DXP. The codes are combined and used to generate a symbol sequence that is modulated synchronously with the host 8-VSB symbols in such a way that ordinary receivers cannot detect their presence but special monitoring and measuring instruments can. Such buried identification signals are also called "RF watermarks."

6.6.1 Transmitter and Network Identification Signaling

Identification of individual transmitters is signaled by causing them to transmit direct sequence buried spread spectrum (BSS) RF watermark signals carrying a unique Kasami code sequence for each transmitter in each network. The symbols of the RF watermark signals are transmitted synchronously with the symbols of the host 8-VSB transmissions, as described in Section 11. The transmitter identification data to be transmitted in the RF watermark signal of each

transmitter shall be communicated to it through the tx_identifier_address, tx_identifier_pattern, and network_identifier_pattern fields of the Distributed Transmission Packet. The twelve bits of tx_identifier_address for a particular transmitter shall precede the total of twenty-seven bits of data of the tx_identifier_pattern and network_identifier_pattern codes plus tx_id_reserved bits included in the DXP for that transmitter. Since the bits of the tx_identifier_address, tx_identifier_pattern, network_identifier_pattern, and tx_id_reserved fields are not sent redundantly within the DXP, each combination of address and patterns shall be sent in three successive DXPs to allow transmitters to apply majority logic techniques before transmitting the code values. The most significant bit of each field shall be sent first. During periods when there is no need to send code patterns to any transmitter, the tx_identifier_address field may be filled with the address of a transmitter non-existent in the network.

The twenty-four bits of the combined tx_identifier_pattern and network_identifier_pattern fields shall represent the initialization value for a shift register code generator of the type shown in Figure 11.1. The initialization value shall be loaded into the shift register code generator during the Data Field and Data Frame Sync data segments, and the code generator shall operate according to the process described in Section 11.

6.6.2 Transmitter Data Signaling Control

To avoid the necessity of a separate remote control system for controlling transmitters in a network, the DXP makes provision for communication of data to the transmitters to support several transmitter control functions. To provide a return channel for status information from the transmitters in a network, the RF watermark signal includes provision for modulation by a slow speed serial data stream inserted at each transmitter. Control of the modulation of the RF watermark signal is enabled by the 1-bit tx_data_inhibit field, which, when set to a value of one, inhibits the modulation of the RF watermark signal by the slow speed serial data. The coding and modulation processes for the slow speed serial data channel are described in Section 11.

6.7 Data Addressed to Individual Transmitters

Within a Distributed Transmission Packet, control data can be individually addressed to up to 16 separate transmitters. If more than 16 transmitters are in a network, DXPs can be sent with control data individually addressed to 16 transmitters at a time. Given the size of the address space and limitations in its use, a total of 4,095 transmitters can be accommodated in a single network. Among control data that can be sent to transmitters individually are the delay offset, the power offset, and the transmitter identifier selection.

6.7.1 Transmitter Addressing

Transmitters within a network shall be individually assigned unique 12-bit addresses. The data within a DXP addressed to each transmitter shall begin with the address of that transmitter, as shown in Table 6.2 and Figure 6.1.

6.7.2 Transmitter Group Indicator

The tx_group_number field shall carry the 8 msb's of the transmitter addresses included in the instance of the DXP. This redundant information may be used by transmitter data processing subsystems to more easily locate the data individually addressed to their associated transmitters and to add reliability to the determination of the addressing of information.

6.7.3 Transmitter Delay Offset

The tx_time_offset fields shall carry the individual offset values for the transmitters associated with the tx_address fields preceding them. The values of tx_time_offset shall be formatted as prescribed in Section 6.5.3.

6.7.4 Transmitter Power Output

Transmitter power output shall be the effective radiated power (ERP), expressed in dB relative to 1 mW (i.e., dBm), from the antenna of the transmitter associated with the tx_address value immediately preceding. The power value shall be sent as 12 bits in the tx_power field in the section of the DXP addressed to the individual transmitter. The most significant 8 bits of tx_power shall carry the integer portion of the power value in the form of a hexadecimal (or binary) number. The least significant 4 bits of tx_power shall carry the fractional portion of the power value in the form of a hexadecimal (or binary) number. The maximum ERP that can be expressed with this method (in decimal notation) is +255.9375 dBm. Use of the range above 5 MW (+96.9897 dBm) is not expected.

Note: Transmitters may or may not implement mechanisms to respond to any or all of the data contained in the tx_power fields.

6.7.5 Transmitter Identifier Levels

The tx_identifier_level fields shall indicate the ratios ("bury ratio") between the average power of the host 8-VSB signals and of the buried spread spectrum signals carrying the transmitter identifier, network identifier, and station signaling codes, as described in Section 6.6.1, for the transmitters identified by the preceding tx_address fields. The bury ratios shall be expressed in dB and shall be indicated by the enumerated values in the leftmost two columns of Table 6.3. The third column in Table 6.3 shows the combined transmitter output SNR at the several bury ratios when a transmitter having a base SNR of 30 dB is used. The fourth column shows the change in theoretical receiver AWGN threshold at the various bury ratios resulting from the combined output SNRs of column 3.

Table 6.3 Transmitter Identifier Bury Ratio

Bit Value	Bury Ratio	Tx SNR w/30	Rx Threshold
000	Identifier Off	30 dB	15.04
001	39dB	29.5	15.05
010	36 dB	29.0	15.07
011	33 dB	28.2	15.11
100	30 dB	27.0	15.18
101	27 dB	25.2	15.32
110	24 dB[1]	23.0	15.63
111	21 dB[1]	20.5	16.30

[1] It is recommended that bury ratios used during normal broadcast operations be chosen so as to result in a transmitter output signal-to-noise ratio (SNR) no less than 27 dB, as specified in ATSC A/64A. A bury ratio of 24 dB, for example, reduces the operating margin at the output of a transmitter from about 12 dB (with the recommended minimum of 27 dB transmitter S/N ratio) to about 7 dB. This may be sufficient reduction to cause some receivers to fail to receive the signal under certain circumstances.

6.7.6 Error Correction Coding

The Distributed Transmission Packet payload shall be protected by Reed Solomon coding within the packet. Since there is no error protection provided within the MPEG-2 Transport Stream structure by itself and since the data in the packet provides synchronization information that cannot be protected by features of a repetitive nature, it is necessary to provide extra protection beyond that normally applied in the transport system between the Distributed Transmission Adapter and the transmitters.

6.7.7 Reed Solomon Coding

The first 164 bytes of the payload of the Distributed Transmission Packet shall be protected by 20 bytes of Reed Solomon (RS) code placed in the last 20 bytes of the packet. The RS code used in the Distributed Transmission Packet shall be a t = l0 (184,164) code. The RS data block size is 164 bytes, with 20 RS parity bytes added for error correction. A total RS block size of 184 bytes is transmitted per Distributed Transmission Packet.

In creating bytes from the serial bit stream, the MSB shall be the first serial bit. The 20 RS parity bytes shall be sent at the end of the Distributed Transmission Packet. The parity generator polynomial and the primitive field generator polynomial shall be as shown in Figure 5 of ATSC A/53 Annex D. The same design as used to RS code the 187-byte data segments in A/53 Annex D may be applied to the Distributed Transmission Packet by stuffing additional bytes having a value of zero at the end of the data to be processed.

7. DISTRIBUTED TRANSMISSION ADAPTER (NORMATIVE)

As shown in Figure 4.1 and described previously, the transmitter synchronization system comprises a Distributed Transmission Adapter at the source end of a studio-to-transmitter link (STL) combined with data processing subsystems at the various transmitters that are capable of responding to the synchronization signals inserted into a standard MPEG-2 Transport Stream by the Distributed Transmission Adapter.

The Distributed Transmission Adapter (DXA) performs the functions of inserting into the TS the Cadence Signal and the fully formed Distributed Transmission Packet described in the previous two major sections of this Standard. It substitutes the necessary DXP data into a packet with the appropriate PID and OM_type values supplied to it as a service by the service multiplexer. It provides the necessary buffering to support the relative timing of the trellis code states and the appearance of the DXP in the Transport Stream. It also provides the necessary buffering to support maintenance of the transmitter frequencies to the necessary precision on both a static and dynamic basis.

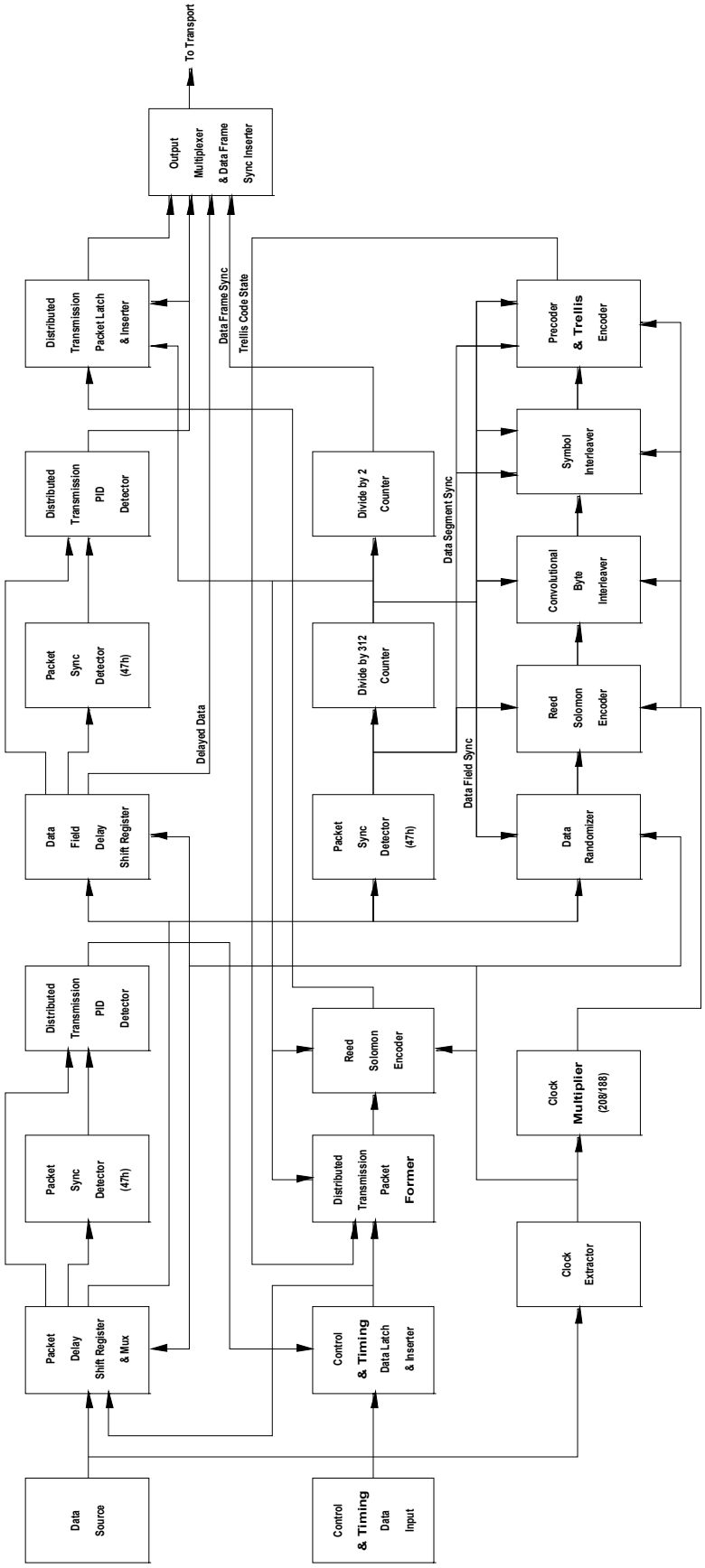
The substitution of DXP data into an appropriate packet takes place in two stages. First, all the data other than the Trellis Code States and the Reed Solomon coding are inserted. The data then in the DXP is next processed through a data processing model along with the other data in the data stream. The second stage of DXP data substitution then inserts the Trellis Code States and the Reed Solomon coding immediately prior to distribution of the DXP to the transmitters. At each transmitter, after stripping the Trellis Code States and the RS coding for purposes of synchronizing the transmitter, default data bit-wise identical to that originally supplied by the service multiplexer is reinserted in their places prior to data processing in the transmitter. The DXP data originally inserted by the DXA in the first stage is broadcast as received through the distribution system. The two-stage process is employed in order to allow broadcasting of the bulk of the DXP data for use by test and measurement equipment.

A conceptual example of a Distributed Transmission Adapter is shown in block diagram form in Figure 7.1. In that figure, only the portions of the Distributed Transmission Adapter necessary to produce the Cadence Signal and the Distributed Transmission Packet are shown. The buffering processes for maintenance of transmitter frequencies are not shown. Also not shown are the mechanisms for determining the information used for transmitter timing adjustment, for transmitter power adjustment, for transmitter mode and identifier control, and for substitution of the reserved bits in the Data Field and Data Frame Synchronization data segments.

7.1 Model Data Processing Subsystem

To achieve the objectives outlined for it, the Distributed Transmission Adapter includes a model of the data processing subsystem of an 8-VSB modulator as defined in ATSC A/53. The data processing subsystem free-runs, establishing the various timing relationships between the input Transport Stream to be transmitted and the several processes that occur in a transmitter. Data can then be extracted from the data processing model, inserted into the Transport Stream, and used to synchronize or slave the equivalent functions in the actual transmitters in the network.

Figure 7.1 Distributed transmission adapter (conceptual) [see *next page*].


To Transport
Output Multiplexer & Data Frame Sync Inserter
Distributed Transmission Packet Latch & Inserter
Data Frame Sync
Trellis Code State
Precoder & Trellis Encoder
Distributed Transmission PID Detector
Divide by 2 Counter
Data Segment Sync
Symbol Interleaver
Packet Sync Detector (47h)
Divide by 312 Counter
Convolutional Byte Interleaver
Delayed Data
Reed Solomon Encoder
Data Field Delay Shift Register
Packet Sync Detector (47h)
Data Field Sync
Data Randomizer
Distributed Transmission PID Detector
Reed Solomon Encoder
Clock Multiplier (208/188)
Packet Sync Detector (47h)
Distributed Transmission Packet Former
Clock Extractor
Packet Delay Shift Register & Mux
Control & Timing Data Latch & Inserter
Data Source
Control & Timing Data Input

7.1.1 All Systems Prior to Symbol Mapping

In Figure 7.1, the bottom row of blocks plus the right-hand three blocks of the middle row comprise most of the data processing elements of a standard 8-VSB modulator subsystem. Missing are the data segment and data field sync insertion blocks, the 313/312 clock multiplier that compensates for the addition of the data field and frame sync data segments, the mapper, and the modulator per se. Included are the packet sync detector, divide by 312 counter, and divide by 2 counter that together establish the relationships between the incoming Transport Stream packets and the Data Field Sync and the Data Frame Sync signals. Also present are all of the data processing elements up through the trellis encoder that allow the establishment of a trellis code trajectory to which all of the trellis encoders in the various transmitters can be slaved.

7.1.2 Establishes References for Transmitters

The model data processing subsystem included in the Distributed Transmission Adapter establishes a timing relationship between each of the included processing functions and the Transport Stream that is to be delivered to the transmitters. It then allows extraction of information about that timing relationship that can be sent to the transmitters along with the Transport Stream data. The information sent to the transmitters allows the equivalent processing functions in the transmitters to adopt the same relationship to the Transport Stream data as was established in the Distributed Transmission Adapter. When all the transmitters adopt the same relationship to the Transport Stream data, they will produce identical symbol outputs for the same Transport Stream data input and thereby effectively become synchronized with one another.

Two synchronization signals are sent from the model data processing subsystem in the Distributed Transmission Adapter to the transmitters: a data frame Cadence Signal, and Trellis Code State information.

7.1.2.1 Data Frame Cadence Signal

The data frame Cadence Signal indicates the timing of the concatenated divide-by-312 and divide-by-2 counters that will cause the insertion of a Data Frame Sync segment into the modulator output. As defined in Section 5.1.3, it indicates the appearance in the modulator output of a Data Field Sync segment with non-inverted middle PN-63 data sequence. At the Distributed Transmission Adapter, the data frame cadence is of random phase with respect to the Transport Stream data; at the transmitters its phase is not random, matching the phase of the data frame cadence established at the Distributed Transmission Adapter.

In the Distributed Transmission Adapter, when the data processing model produces a Data Frame Sync signal that, in a transmitter modulator, would result in the transmission of a Data Frame Sync data segment, a Cadence Signal shall be substituted for the ordinary packet header in the output Transport Stream by the Output Multiplexer & Data Frame Sync Inserter.

7.1.2.2 Trellis Code State Information

The Trellis Code State information carries the states of all three memory elements of each of the twelve conceptual trellis coders used in the data processing subsystem of the modulator. As defined in Section 6.2.1, the 36 bits of information indicate the states of the trellis coders at the beginning of the first data segment following the next occurrence of a Data Field Sync data segment. At the Distributed Transmission Adapter, the trellis code state is random with respect to the Transport Stream data; at the transmitters its state is not random, matching the state of the trellis encoder established at the Distributed Transmission Adapter.

In the Distributed Transmission Adapter, the Data Field Delay Shift Register delays the entire Transport Stream by a period of one data field. The delay allows the state of the trellis coder at the end of a data field to be inserted into a Distributed Transmission Packet contained within the same data field. The Data Field Delay Shift Register also provides the ability to look ahead at the data before it is output to the Output Multiplexer in order to anticipate various events.

7.2 Distributed Transmission Packet Formation

As previously described, the formation of the Distributed Transmission Packet takes place in two stages within the Distributed Transmission Adapter. First, a packet with the appropriate PID and OM_type values and stuffed with the pre-defined payload data sequence is received from the service multiplexer of the upstream system. All of the data other than the trellis code states and the Reed-Solomon error correcting codes are inserted into the packet at the beginning of the DXA processing chain. The packet is then passed through the data processing model already described and contributes to the formation of the trellis codes. When the packet appears in the delayed output of the DXA, the trellis code and Reed Solomon information are inserted to complete the packet prior to its distribution to the transmitters. How all this takes place is described in this section.

7.2.1 Distributed Transmission Adapter Processing

The top row in Figure 7.1 plus the left-hand four blocks of the middle row include the additional processing elements that are necessary to convert a packet having the PID and OM_type values reserved for transmitter control into a Distributed Transmission Packet. On the top row, they are two shift registers, one having a delay of one packet period and one having a delay of one data field period, two packet sync detectors, two detectors for the PID and OM_type values reserved for transmitter control, a latch for trellis code state data and an inserter to output that data to a multiplexer at the correct time, and an output multiplexer capable of replacing the data in the payload of the designated packet and of replacing the packet sync word at the designated times. On the middle row, they are the source of control and timing data, a control and timing data latch and inserter, a Distributed Transmission packet former, and a Reed Solomon encoder. The operations of the respective additional processing elements are discussed Section 7.2.3.

7.2.2 Distributed Transmission Packet Pre-Processing Payload

Because the same data must be processed by the data processing subsystems in the Distributed Transmission Adapter and in the several transmitters in order to establish and maintain synchronization, it is necessary to assure that, when data is substituted in the delivery channel, the data that was processed at the Distributed Transmission Adapter is reinserted at the transmitters. The way to meet this requirement is to use known values at the Distributed Transmission Adapter and at the transmitters for the data that will be substituted in the delivery channel. Thus, the payload data of the packets identified by the PID and OM_type values reserved for transmitter control shall be as specified in this section when delivered to the Distributed Transmission Adapter for processing. Specified portions of the packet are returned to their initial states prior to data processing at the transmitters, and, when such restoration of the initial states is required, the patterns defined in this section shall be followed.

7.2.2.1 Fixed Value Packet Payload Values

The payloads of the packets identified by the PID and OM_type values reserved for transmitter control shall have fixed values when delivered to the Distributed Transmission Adapter. Most or

all of this data will be replaced in the DXA prior to delivery to the transmitters. During transport between the Distributed Transmission Adapter and the transmitters, the payloads shall carry the transmitter control data values defined in Section 6. Upon processing for transmission, the original, fixed payload data values shall be substituted for those portions of the transmitter control data carried during transport that are not to be transmitted.

7.2.2.1.1 Alternating Values

The fixed values of payload data used for data processing in the Distributed Transmission Adapter and in the transmitters of packets having the PID and OM_type values reserved for transmitter control shall consist of alternating bytes of data representing the values 0xAA (10101010) and 0x55 (01010101). The value 0x55 shall appear in the second payload byte and in every even-numbered byte thereafter until the end of the packet. The value 0xAA shall appear in the third payload byte and in every odd-numbered byte thereafter until the next to last byte of the packet. (The first payload byte carries the OM_type field.)

7.2.3 Distributed Transmission Packet Payload Substitution

As described previously, substitution of the payload of the packet reserved for transmitter control takes place in two stages. The first stage occurs in the three blocks to the right of the Data Source in the top row of Figure 7.1 and in the first block to the right of the Control and Timing Data Input in the second row. In the top row, the data is fed through a Packet Delay Shift Register and Multiplexer. Connected to the shift register so as to look ahead into its contents are a Packet Sync Detector and a Distributed Transmission PID Detector. When the latter two devices detect a packet sync word and the appropriate PID and OM_type values, they trigger the Control and Timing Data Latch and Inserter on the second row of Figure 7.1. It, in turn, inserts data back into the Packet Delay Shift Register and Multiplexer. That data replaces all the necessary payload data, other than the trellis code state data and the Reed Solomon coding data, to form a Distributed Transmission Packet. The output of the Packet Delay Shift Register and Multiplexer is then fed to the blocks in the right half of Figure 7.1 for the second stage of data insertion.

When the Control and Timing Data Latch and Inserter forms its portion of the payload of the DXP, it sends a copy of it to the Distributed Transmission Packet Former. That device adds the Trellis Code State data to form a complete Distributed Transmission Packet except for the Reed Solomon coding. Its output then goes to a Reed Solomon coder, where the necessary error correction coding is calculated and added to the packet. The packet is then stored in the Distributed Transmission Packet Latch and Inserter on the right end of the top row of Figure 7.1.

7.3 Distributed Transmission Packet Insertion Rate

The Distributed Transmission Packet insertion rate into the Transport Stream will depend upon a number of factors. It shall be inserted at the rates and under the conditions described in this section.

7.3.1 Minimum Insertion Rate

No minimum insertion rate for Distributed Transmission Packets is specified. The minimum insertion rate should be set for each system based upon a balance of the overhead data capacity required for transmitter synchronization and the recovery time for any given transmitter following an error in the synchronization process. By way of example, an insertion rate of one DXP per second would utilize approximately 0.0078 percent of the overall data capacity of the channel.

7.3.1.1 Service of Data Multiplexer

The insertion of the transmitter control packets having the fixed payload described above that will be turned into Distributed Transmission Packets by the Distributed Transmission Adapter shall be a service provided by the Service Multiplexer or similar device upstream of the Distributed Transmission Adapter. This requirement is necessary to assure the occurrence of the packets at the desired insertion rate.

7.3.1.2 DXA Packet Insertion with No Input

When no input is received by the Distributed Transmission Adapter from an upstream service multiplexer, the DXA shall create at its input a stream of MPEG-2 Transport Stream null packets, having a bit rate of 19.39…Mb/s as specified precisely in A/53A Annex C. It shall insert into that stream at a rate of approximately one per second transmitter control packets suitable for conversion to Distributed Transmission Packets. The requirement noted in this paragraph is for the purpose of keeping the Distributed Transmission System operating and synchronized even when there is no input to the DXA.

7.3.2 Maximum Insertion Rate

The maximum insertion rate for Distributed Transmission Packets shall be no greater than one packet of every 312 packets in the Transport Stream; i.e., there shall be a minimum of 24.2 ms between the start of one DXP and the next. This ensures that there will be no more than one DXP per transmitted data field.

7.4 Distributed Transmission Packet Payload Substitution

When packets having the PID and OM_type values reserved for transmitter control appear in the Transport Stream, they shall have their payloads substituted by the Distributed Transmission Adapter with the data necessary to form a Distributed Transmission Packet. The data substitution is done in such a manner as to process all the data but the trellis code state data and the Reed Solomon ECC through the data processing model. This includes them in the formation of the trellis code trajectory and allows them to be broadcast by the transmitters.

Upon entry of the packets having the transmitter control PID and OM_type values into the DXA, the stuffing code (alternating 0xAA and 0x55 bytes, as described in Section 7.2.2.1) shall be replaced in the appropriate places with all of the information to be transported in the DXP except for the 7^{th} through the 18^{th} and the 169^{th} through 188^{th} bytes of the packet. Those bytes will carry the trellis code states and the Reed Solomon ECC, respectively, and will be substituted later in the process. Any bytes not carrying information in any particular instance of the DXP shall retain the stuffing code pattern that originated in the service multiplexer (or that was created by the DXA in the absence of input).

In the example DXA design of Figure 7.1, the substitution for the stuffing pattern of the data to be sent to the transmitters (other than the trellis code states and the Reed Solomon ECC) occurs in the Packet Delay Shift Register and Multiplexer near the left end of the top row. The substitution takes place when the Packet Sync Detector and the Distributed Transmission PID Detector, just to the right of the packet delay block, determine that a packet having the appropriate PID and OM_type values is contained in the shift register in the correct position. At that time, the data stored in the Control and Timing Data Latch and Inserter is substituted for the stuffing pattern. It then proceeds along with the existing header for the packet in the normal sequence of packets through the remainder of the data processing within the DXA. Since the data substituted into the packet at this point passes through the portion of the DXA data processing

that includes the trellis code generation, the transmitters must transmit such substituted data in order to result in matching trellis code trajectories, thereby keeping all the transmitters locked together.

Again in the example DXA of Figure 7.1, the trellis code states and the Reed Solomon ECC data are substituted into the 7th through the 18th and the 169th through the 188th bytes, respectively, of the DXP near the end of the DXA data processing chain. The trellis code states and Reed Solomon ECC are stored in the Distributed Transmission Packet Latch and Inserter in the upper right corner of the figure. The substitution takes place when the Packet Sync Detector and the Distributed Transmission PID Detector, just to the right of the Data Field Delay Shift Register in the middle of the top row, determine that a packet having the appropriate PID and OM_type values is contained in the shift register in the correct position. At that time, the Output Multiplexer and Data Frame Sync Inserter substitute the data stored in the Control and Timing Data Latch and Inserter for the stuffing pattern in the appropriate positions within the packet. Alternatively, the entire payload of the DXP can be stored in the Distributed Transmission Packet Latch and Inserter and then substituted for the data in the packet. This latter approach will overwrite the data that was previously substituted at the beginning of the DXP processing, but the overwriting will be with the same data. The trellis code states and Reed Solomon ECC data will be part of the substituted information. Any portions of the packet not actually containing data to be substituted will have to retain or be stuffed again with the correct stuffing pattern.

7.5 Transport Stream Output Frequency Stability and Accuracy

The Distributed Transmission Adapter shall contain adequate buffering so that its output complies with the frequency stability requirements of SMPTE 310M despite instantaneous frequency changes at its input extending from one end of the SMPTE 310M frequency tolerance range to the other. That is, its output frequency shall remain accurate to within ±2.8 ppm, with its frequency changing by no more than 0.028 ppm per second, when its input instantaneously changes from –2.8 ppm error to +2.8 ppm error, or vice versa.

When no input is received by the Distributed Transmission Adapter from an upstream service multiplexer, the DXA is required to create a stream of MPEG-2 Transport Stream packets as described Section 7.3.1.2. The Transport Stream output frequency stability and accuracy of the DXA shall be maintained as described in the preceding paragraph under such conditions of no input.

8. TRANSMITTER SYNCHRONIZATION (NORMATIVE)

As shown in Figure 4.1 and described previously, the transmitter synchronization system comprises a Distributed Transmission Adapter (DXA) at the source end of a studio-to-transmitter link (STL) combined with data processing subsystems at the various transmitters that are capable of responding to the synchronization signals inserted into a standard MPEG-2 Transport Stream by the DXA.

The Distributed Transmission Adapter is described in Section 7. The data processing subsystem at each transmitter, in addition to the normal processes of an 8T-VSB transmitter, performs the functions of responding to the Cadence Signal and to the Distributed Transmission Packet (DXP) carried in the TS and described in Sections 5 and 6, respectively. The transmitter data processing subsystem substitutes for certain of the DXP data, in packets with the assigned PID and OM_type values, the fixed data pattern that was replaced in the Distributed Transmission Adapter. This subsystem provides the necessary buffering of the trellis code states to support the slaving of the trellis coders at the appropriate times.

The channel coding processes of a typical 8T-VSB modulator are shown in block diagram form in Figure 8.1. In that figure, only the portions of the subsystem necessary for ordinary data and signal processing and to respond to the Cadence Signal and the Distributed Transmission Packet are shown. Not shown are the mechanisms for extracting and applying the information from the DXP used for transmitter timing adjustment, for transmitter power adjustment, for transmitter mode and identifier control, and for substitution of the reserved bits in the Data Field and Data Frame Synchronization data segments.

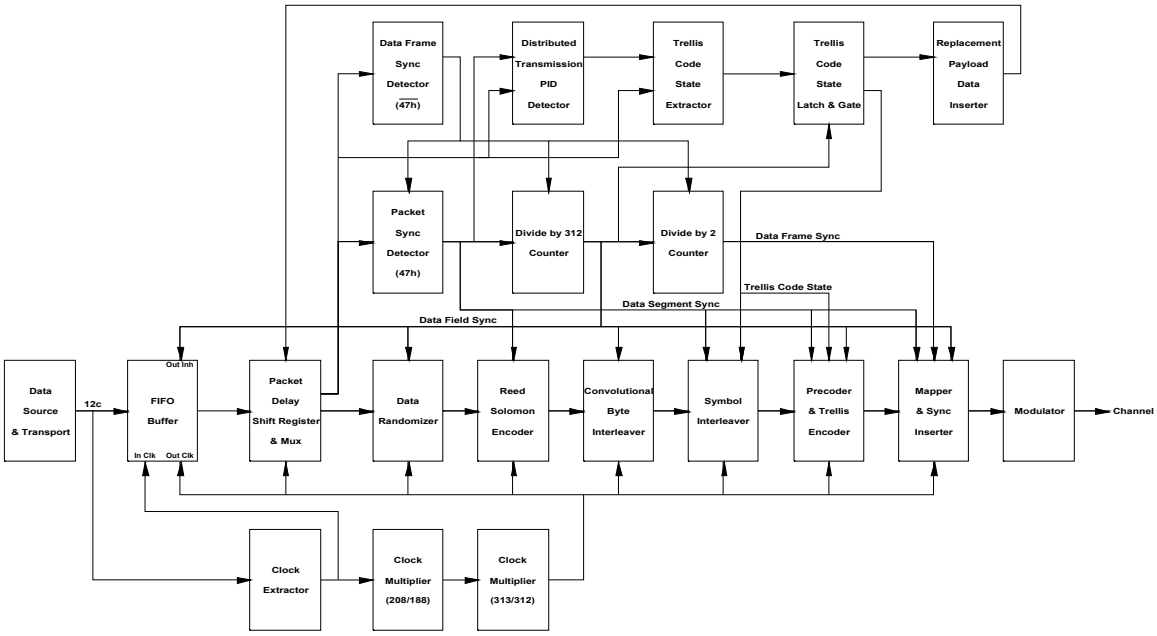


Figure 8.1 Synchronized 8-VSB transmitter channel coding.

8.1 Standard Modulator Functions

Included in the synchronized modulator system of Figure 8.1 are all the standard functions of an 8T-VSB modulator as defined in ATSC A/53 Annex D as well as those necessary to make such a modulator operate properly. The bottom three rows of Figure 8.1 represent the standard functionality with the addition of one block required for the synchronization processes. The bulk of the added functions for the synchronization processes are contained in the top row of the diagram.

8.1.1 Data Processing

The basic data processing functions of an 8T-VSB modulator are carried out in the next to the bottom row of Figure 8.1. They include a FIFO buffer to adjust the data rate to compensate for the insertion of data field and data frame sync data segments, the data randomizer, the Reed Solomon encoder, the convolutional byte interleaver, the symbol interleaver, the precoder and trellis encoder, and the mapper and sync inserter. Supporting these functions are the clock extractor and two clock multipliers (208/188 and 313/312) shown in the bottom row of the diagram. Also supporting the standard functionality are the three blocks of the third row from the bottom, namely, the packet sync detector, divide by 312 counter, and divide by 2 counter.

Without the additional functions included in the top row of the diagram and the added block in the next to bottom row, the modulator shown in Figure 8.1 would produce standard 8T-VSB signals in the normal unsynchronized way.

8.1.2 Signal Processing

Also included in Figure 8.1 is the normal signal processing portion of an 8T-VSB modulator. It comprises part of the mapper plus the modulator shown on the right side of the next to bottom row of the diagram. Given the symbols from the precoder and trellis encoder, the mapper and modulator produce a fully modulated radio frequency signal that can be upconverted by the transmitter to the assigned channel of the digital television station.

8.2 Data Frame Cadence Synchronization

Two types of synchronization are required in modulators for Distributed Transmission. One is the alignment of all the repetitive functions that are reset or are set to known states periodically in the modulation process. The processes that must be reset or set to known states are the data randomizer, the Reed Solomon encoder, the convolutional byte interleaver, the symbol interleaver, and certain aspects of the precoder and trellis encoder operation. The time alignment of the necessary processes is enabled through periodic inclusion in the stream of the Cadence Sync word, the extraction of that sync word, and its use to set the data frame sync segment timing.

8.2.1 Cadence Sync Detection

Following the FIFO buffer at the left side of the next to bottom row is a packet delay shift register and multiplexer. It serves several purposes in the synchronization of both the repetitive processes and the stochastic processes. Fundamentally, it provides a fixed delay of 188 bytes (one MPEG-2 packet) and allows access to the contents of each packet prior to its entry into the normal data processing portion of the modulator. Effectively, it allows looking ahead into data that has not yet been processed and permits modifying the data before its entry into the normal data processing functions.

For synchronizing the repetitive functions in the modulator data processing subsystem, there are two detectors that examine the MPEG-2 packet sync words at the output of the packet delay shift register. The normal packet sync detector is at the left end of the next to top row. It examines the stream for values of 0x47, which is the standard MPEG-2 packet sync word. When it detects a packet sync word, it triggers the data segment sync function, time-aligning all the data processing functions that recycle at data segment periodicity. It also triggers the divide-by-312 counter and, through it, the divide-by-2 counter that establish the timing of the Data Field and Data Frame Sync segment insertion.

The additional detector used in synchronizing distributed transmitters is at the left end of the top row. It examines the stream for values of 0xB8, the Cadence Sync word, which is the bit-by-bit inverse of the standard MPEG-2 packet sync word. The value 0xB8 is inserted in the stream by the Distributed Transmission Adapter at times when the value 0x47 would normally appear to indicate the start of an MPEG-2 packet. Only occurrences of the value 0xB8 that appear in the stream at times when they are expected should be interpreted as instances of the Cadence Sync word; i.e., in place of every 624th packet sync word.

8.2.2 Data Frame Synchronization

When a Cadence Sync word is detected, several things happen. First, the packet sync detector is triggered to indicate the start of an MPEG-2 packet. This will result in triggering the data segment sync function as described in Section 8.2.1. All of the data processing functions that are normally time aligned by the packet sync shall be aligned similarly by the Cadence Sync. The timing mechanism used to control insertion of Data Field Sync and Data Frame Sync data segments shall be controlled by the occurrence of the Cadence Sync (e.g., the two counters in the next to top row of Figure 8.1 are reset by detection of the Cadence Sync word). A Data Frame Sync data segment shall be emitted immediately before emission of the data segment containing the beginning of the MPEG-2 packet carrying the Cadence Sync word at its start.

As defined in Section 5.1.3, appearance of the Cadence Sync word in the MPEG-2 Transport Stream transported to the transmitters corresponds with the output from the transmitters of the Data Field Sync data segment having no inversion of the middle PN-63 sequence; i.e., the Data Frame Sync data segment.

8.3 Distributed Transmission Packet Payload Replacement

When the Distributed Transmission Adapter received the packet from which it created the Distributed Transmission Packet, the values of the words in the packet were known. Those words were then replaced in two stages with the information to be communicated by the Distributed Transmission Packet. The first stage replaced certain words with data that are to be broadcast. The packet was then processed by the data processing model that exists in the DXA to derive the trellis coder states to which the transmitters are to be slaved. The second stage replaced words that carry the trellis code state and Reed Solomon ECC data to the transmitters. At the transmitter, it is necessary to restore the known values of those words in the DXP that carry the trellis code state and Reed Solomon ECC data before they are data processed so that the same trellis code states are obtained as at the Distributed Transmission Adapter.

The process begins with a Distributed Transmission Packet PID detector. Each time a packet sync word or Cadence Sync word is detected, the PID detector is triggered to check for the occurrence of the PID and OM_type values assigned to the Distributed Transmission Packet. It looks into the Packet Delay Shift Register at the appropriate location relative to where the packet sync word or Cadence Sync word will be when detected.

When the DXP PID and OM_type are detected, the Trellis Code State Extractor to the right of the Distributed Transmission PID Detector will capture all of the needed information from the Distributed Transmission Packet and store it in appropriate latches and registers. In Figure 8.1, only the Trellis Code State Latch and Gate is shown; similar storage devices are used for capturing the other information present in the packet.

8.3.1 Fixed Value Packet Payload

Once the information in the Distributed Transmission Packet has been extracted from the packet and stored as necessary, certain of the information in the packet is replaced. At the right end of the top row is the Replacement Payload Data Inserter. Fundamentally, this block stores or creates a repeating pattern of words having the values 0xAA and 0x55, as defined in Section 7.2.1.1. When the Distributed Transmission Packet is recognized and once the information in that packet has been extracted, the contents of the 7th through the 18th and the 169th through 188th of the 188 bytes of the packet shall be replaced by the defined pattern of words (as, for example, by the Replacement Payload Data Inserter and the Packet Delay Shift Register and Multiplexer in

Figure 8.1). In this way, the packet is restored to its state after the first stage of processing in the DXA—the state in which it was when it entered the data processing model of the DXA.

8.3.2 Matches Pre-Processing Value

The payload inserted into the Distributed Transmission Packet at the transmitter shall exactly match the values that were replaced in the second stage at the Distributed Transmission Adapter. The result is that the signal that is processed by the transmitter modulator is exactly the same as that which was processed by the data processing model in the Distributed Transmission Adapter.

8.3.3 Traverses Transmitter Modulator

The Distributed Transmission Packets traverse the transmitter modulator and are transmitted in exactly the same way as are all the other packets. By this mechanism, when the trellis coder is synchronized with the trellis coder in the Distributed Transmission Adapter, after the first synchronization sequence and if there has been no interruption in the signal to the transmitter, there will be no modification of the values in the trellis coder. Instead the values at both ends of the transport system will match and will continue to run in lock step.

8.4 Trellis Code Slaving

In order to put the precoders and trellis encoders of all the transmitters in a network in the same states at the same time, it is necessary to "jam sync" them to the trellis coder model in the Distributed Transmission Adapter. By this mechanism, they will be set to matching states upon startup, and they will be maintained in matching states while running. Only upon occurrence of an error in the transport system to a transmitter or in the event of a change being made in the operational timing of a transmitter will it be necessary to resynchronize a transmitter during continued operation.

8.4.1 Trellis Code State Extraction

As previously described, when the PID and OM_type values assigned to the Distributed Transmission Packet appear in the MPEG-2 Transport Stream, the Trellis Code State values contained in that packet shall be extracted and stored until needed (as, for example by the Trellis Code State Extractor and the Trellis Code State Latch and Gate in Figure 8.1).

8.4.2 Trellis Code State Slaving

Each time a Distributed Transmission Packet is received from the transport system, the Trellis Code State data is stored in the Trellis Code State Latch and Gate through operation of the Trellis Code State PID Detector and the Trellis Code State Extractor. When the next Data Field Sync occurs, the Trellis Code State Latch is checked for the presence of current Trellis Code State data. If current trellis_code_state data is present, it shall be used to set the states of the precoder and trellis encoder storage elements during the Data Field Sync data segment. Then, when the first data segment following Data Field Sync starts, its trellis encoders will be in the same states as were those of the data processing model in the Distributed Transmission Adapter when it processed the same Transport Stream data.

The operation of an individual Synchronized Precoder and Trellis Encoder is shown in Figure 8.2. The operation of the associated Synchronized Trellis Code Interleaver is shown in Figure 8.3. The processes described for Figures 6.2 and 6.3 are reversed in Figures 8.2 and 8.3, and the 36 bits of Trellis Code State data are inserted in 3-bit groups into the 12 related Precoders and Trellis Encoders when the Data Field Sync indicates the correct instant for doing

so. The insertion takes place through control of the multiplexers on the inputs of the storage elements of each Precoder and Trellis Encoder. (Note that the designations of signals in Figure 8.2 match those of A/53, Annex D, Figure 7.8.)

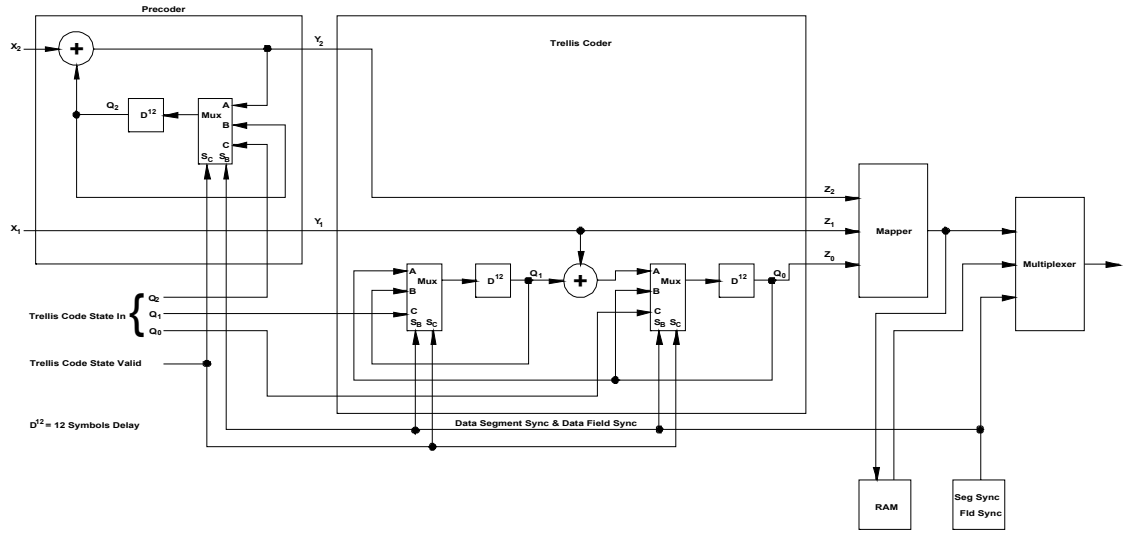


Figure 8.2 Synchronized precoder, Trellis coder, and mapper.

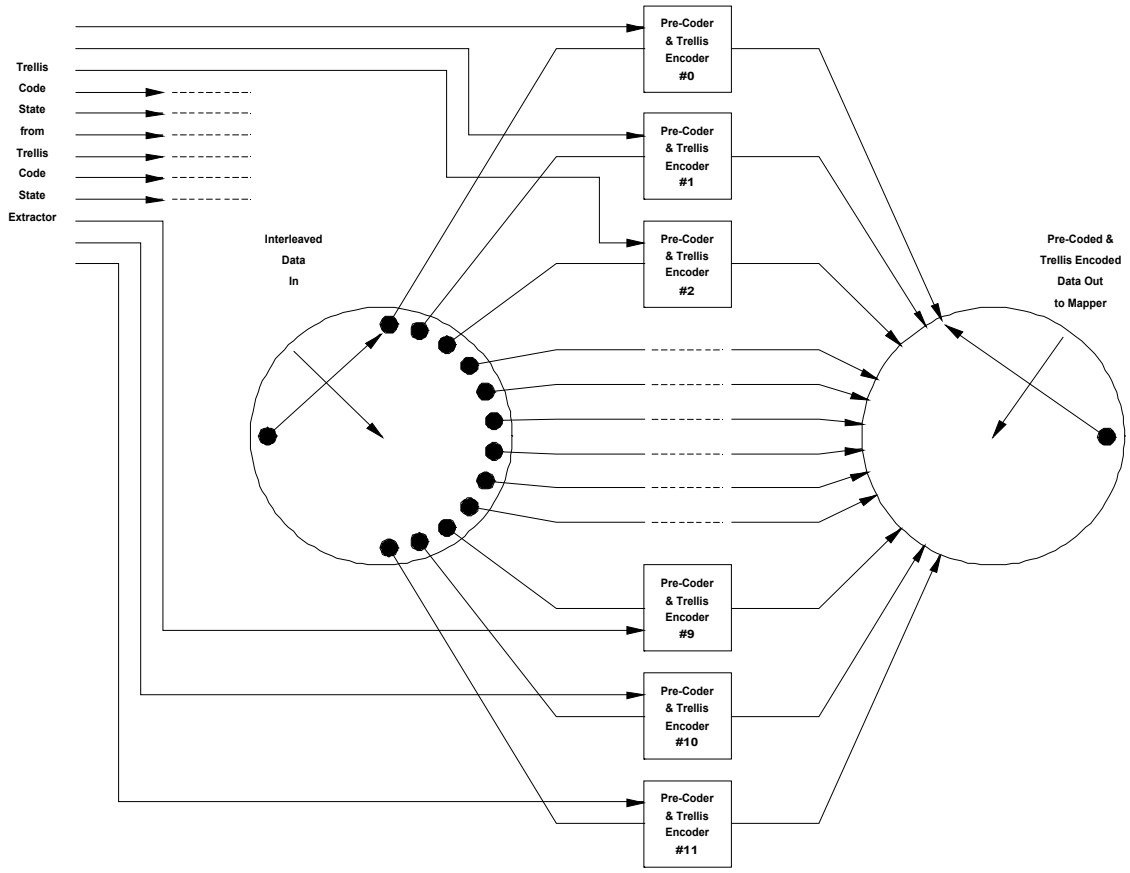


Figure 8.3 Synchronized Trellis code interleaver.

9. TRANSMITTER MODE CONTROL (NORMATIVE)

Provision is made in the Distributed Transmission Packet for inclusion of Transmitter Mode Control bits that both control the mode of the transmitters and replace the bits that are used to signal the transmitter operating mode to receivers. While not detailed in a diagram, the operation of the Mode Control bits at each transmitter is described in this Section. The extraction methods and application timing explained also apply to the Reserved bits that are transmitted in the Data Field Sync data segment and that are carried to the transmitters in the Distributed Transmission Packet.

9.1 Mode Control Data Extraction

The extraction from the Distributed Transmission Packet of the transmitter_mode_control bits and the dfs_reserved bits functions in the same way as the extraction of the Trellis Code State data. That is, when the Distributed Transmission PID Detector locates a Distributed Transmission Packet, a Mode Control Data Extractor, parallel in function to the Trellis Code State Extractor described earlier, captures the transmitter_mode_control data. It does so by collecting the transmitter_mode_control data from the Packet Delay Shift Register and Multiplexer before certain of the payload data in the packet is replaced with the standard data fill pattern. The data so captured is stored in a

register until needed at the time of the next Data Field Sync data segment. The dfs_reserved bits are captured and stored in a register in like manner.

9.2 DFS Mode Data Derivation

The transmitter_mode_control bits to be transmitted in the Data Field Sync and Data Frame Sync data segments shall be extracted from the locations within the Distributed Transmission Packet defined in Table 6.2 and Figure 6.1. They shall be unpacked from the respective words carrying them as defined in Figure 6.4 and Section 6.3.

9.3 Transmitter State Change Timing

When a change occurs in the transmitter_mode_control bits as sent to the transmitters from the Distributed Transmission Adapter, the new transmitter_mode_control bits shall be inserted into the next Data Field Sync or Data Frame Sync data segment to be transmitted after receipt of the new transmitter_mode_control information in the Transport Stream. The transmitter shall delay adoption of the new mode for one Data Field period. It shall transition to the new mode upon the occurrence of the next Data Field Sync or Data Frame Sync data segment following the Data Field Sync or Data Frame Sync data segment in which the updated transmitter_mode_control bits are first transmitted.

9.4 DFS Reserved Data Derivation

The dfs_reserved bits to be transmitted in the Data Field Sync and Data Frame Sync data segments shall be extracted from the locations within the Distributed Transmission Packet defined in Table 6.2 and Figure 6.1. They shall be unpacked from the respective words carrying them as defined in Figure 6.4 and Section 6.3.

9.5 Transmitter Reserved Data Change Timing

When a change occurs in the dfs_reserved bits as sent to the transmitters from the Distributed Transmission Adapter, the new dfs_reserved bits shall be inserted into the next Data Field Sync or Data Frame Sync data segment to be transmitted after receipt of the new Mode Control information in the Transport Stream. Should the dfs_reserved bits take on any meaning that affects the transmitter operation, the transmitter shall delay adoption of the new characteristics for one Data Field period. It shall transition to the new characteristics upon the occurrence of the next Data Field Sync or Data Frame Sync data segment following the Data Field Sync or Data Frame Sync data segment in which the updated dfs_reserved bits were first transmitted.

10. TRANSMITTER TIMING ADJUSTMENT (NORMATIVE)

The information sent collectively to all transmitters in a network and sent individually to each transmitter is described in Section 6.5 and Figure 6.6. When a transmitter receives a Distributed Transmission Packet, it shall calculate the time of emission for its signals based upon the timing information sent to it from the Distributed Transmission Adapter.

10.1 Data Frame Start Time Reference

In order for each transmitter to properly calculate the time of emission for its signals, an appropriate time reference is required and the emission time of a defined point in the transmitted symbol stream must be measured with respect to that time reference. The emission time to be measured shall be that of the leading edge (zero crossing of the +5 to –5 transition) of the first Data Segment Sync following the first Data Field Sync or Data Frame Sync data segment that

follows arrival at the transmitter of the Distributed Transmission Packet carrying the timing information.

10.1.1 External Precision Time Reference

The external time reference shall be a source that is available with an accuracy of 50 ns or better at all transmitter locations. The preferred time reference is derived from the Global Position System (GPS) satellite navigation system.

10.1.1.1 1 Second Ticks

The one-second ticks of the external time reference shall be used to align the timing of the respective transmitters relative to one another and to the signals from the Distributed Transmission Adapter.

10.2 Data Field Start Time Alignment

As defined in Section 10.1, the time of emission of the start of the next data field following arrival of the Distributed Transmission Packet shall be set according to the information sent to all transmitters and to each individual transmitter, as defined in Section 6.5 and Figure 6.6. A change in the delay between the arrival of data in the Transport Stream and its emission is disruptive to reception because the addition or deletion of symbols is required, thereby breaking the framing structure of the signal. Consequently, transmitters shall not alter their delay times (TX Delay in Figure 6.6) until a change of at least 5 symbols (equal to approximately 1/2-microsecond) is required. Transmitter settings to allow accumulation of longer required changes in TX Delay before making such changes are expressly permitted.

10.2.1 STS Plus Max Delay Plus Offset

As defined in Section 6.5 and Figure 6.6, the time of emission of the reference point in the symbol stream shall be the sum of the Synchronization Time Stamp (STS) plus the Maximum Delay (MD) plus the individual Transmitter Time Offset for the reference point in the symbol stream first following the occurrence in the Transport Stream of a Distributed Transmission Packet with a Transmitter Time Offset value addressed to the particular transmitter. In order to maintain the appropriate time of emission between DXPs with time offset information addressed to it, a transmitter should calculate the difference between the time of arrival of the reference point in the data stream and the time of emission of the reference point in the symbol stream calculated as described previously. Until a new delay value is calculated, that difference value should be used to set the delay time for all succeeding data from arrival in the Transport Stream until its emission.

Time of emission shall apply to the time that the reference symbol leaves the antenna. It may be necessary to calculate the time delay through the transmission system from the output of the modulator, through the upconversion and amplification stages, through the output filters and other RF equipment, through the transmission lines, and to the antenna. Equipment used to automatically adjust the time of emission shall have the capability to accept the input of a value to indicate the delay in the transmission system following the measurement point of the emission timing if that point is not at the antenna.

11. IDENTIFICATION CODE GENERATION AND TRANSMISSION (NORMATIVE)

As described in Section 6.6, Transmitter Identification and Signaling, provision is made to individually identify transmitters through the use of an “RF watermark” so as to enable system

monitoring and measurements. Such identification can be accomplished without requiring the shutting down of transmitters in order to determine which one or ones are contributing to the signals received at any given location. Moreover, the channel impulse response components of each transmitter received at a given location can be determined. This determination can allow in-service system adjustments of such characteristics as power levels and delay offsets.

As provided in the DXP data that is addressed to each transmitter, it is possible to set the insertion level of the buried spread spectrum (BSS) RF watermark signal in use at any time, including turning it off. The insertion levels are chosen to allow operation from well below the normal noise floor of host 8-VSB transmitters up to levels that perhaps could cause some receivers to lose the ability to recover the signal. Obviously, the higher levels should only be used in out-of-service testing. The impacts of the various levels on typical receiver performance will be documented in a future application guide to this Standard.

11.1 Code Generation

The buried spread spectrum RF watermark signal shall carry a Kasami code sequence that is transmitted repeatedly throughout the period when it is enabled in the transmissions from the particular transmitter with which it is associated. The code shall be generated in a group of three shift registers having specified feedback arrangements and set to known values at specified times. The shift registers shall be clocked at the symbol rate of the host 8-VSB signal. Provision is made for modulation of the RF watermark signal by a slow speed serial data signal to permit return data transmission for remote control and other purposes. Provision also is made for future enhancements in the code generation methods.

11.1.1 Multiple Shift Registers

The code transmitted by the BSS RF watermark signal shall be generated by a group of 3 shift registers having lengths, feedback paths and summing functions as defined in Figure 11.1. The shift registers also shall have inputs through which they can be preloaded upon the occurrence of an enabling pulse. The output of the set of shift registers shall be sent to the equivalent of a 2-VSB modulator for transmission with the 8-VSB host signal.

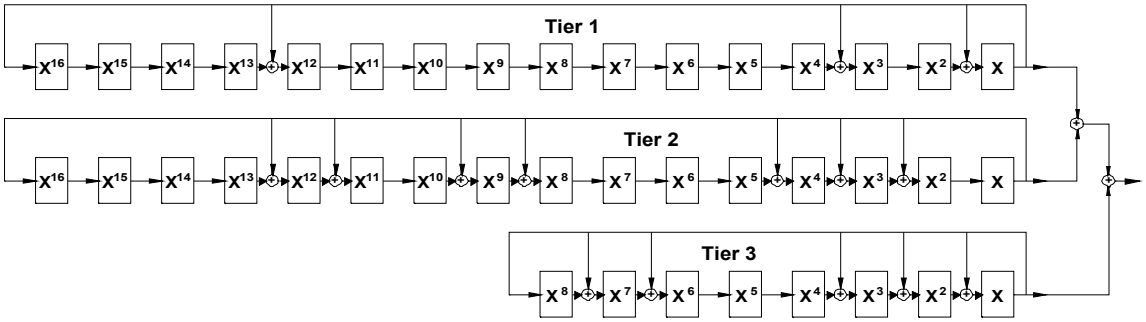


Figure 11.1 Identification code generator (Kasami sequences).

The generator polynomials used in the respective tiers of the sequence generator shall be:

Tier 1 Generator Polynomial $G_{(16)} = X^{16} + X^{12} + X^3 + X + 1$

Tier 2 Generator Polynomial $G_{(16)} = X^{16} + X^{12} + X^{11} + X^9 + X^8 + X^4 + X^3 + X^2 + 1$

Tier 3 Generator Polynomial $G_{(8)} = X^8 + X^7 + X^6 + X^3 + X^2 + X + 1$

11.1.2 Clock Rate and Phase

The clock applied to the shift registers shown in Figure 11.1 shall operate at the symbol clock rate of the host 8-VSB signal, as defined in ATSC A/53B, Annex D, Section D.4. The clock rate thus shall be approximately 10.76… MHz. The clock phase shall be set so that BSS symbols are generated in phase with the symbols of the host 8-VSB signal as defined in Section 11.2.2.

11.1.3 Preloaded Values

The values preloaded into the shift registers of Figure 11.1 shall be those values sent in the DXP in the tx_identifier_pattern, and network_identifier_pattern fields addressed to each particular transmitter. In addition, one shift register shall be preloaded with a fixed value. The values shall be preloaded during Data Field Sync and Data Frame Sync data segments.

The shift register in Tier 1 of the Kasami code sequence generator of Figure 11.1 shall be preloaded with a value of 1 in the X stage and 0 in all the other stages. The twelve bits of the tx_identifier_pattern shall be preloaded into the X^{16} through X^5 stages of the Tier 2 shift register of the code sequence generator; the msb shall be preloaded into the X^{16} stage and the lsb into the X^5 stage. The four msb's of the network_identifier_pattern shall be preloaded into the X^4 through X stages of theTier 2 shift register of the code sequence generator; the msb shall be preloaded into the X^4 stage and the third msb into the X stage. The eight lsb's of the network_identifier_pattern shall be preloaded into the X^8 through X stages of theTier 3 shift register of the code sequence generator; the fourth msb shall be preloaded into the X^8 stage and the lsb into the X stage.

The preloading of the shift registers of the code sequence generator is summarized in Table 11.1. In the table, values denoted as "t" are the respective bits of the tx_identifier_pattern field, and those denoted as "n" are the respective bits of the network_identifier_pattern field.

Table 11.1 Code Sequence Generator Preloading

	Tier 1	Tier 2	Tier 3
X^{16}	0	t^{12}	—
X^{15}	0	t^{11}	—
X^{14}	0	t^{10}	—
X^{13}	0	t^{9}	—
X^{12}	0	t^{8}	—
X^{11}	0	t^{7}	—
X^{10}	0	t^{6}	—
X^{9}	0	t^{5}	—
X^{8}	0	t^{4}	n^{8}
X^{7}	0	t^{3}	n^{7}
X^{6}	0	t^{2}	n^{6}
X^{5}	0	t^{1}	n^{5}
X^{4}	0	n^{12}	n^{4}
X^{3}	0	n^{11}	n^{3}
X^{2}	0	n^{10}	n^{2}
X	1	n^{9}	n^{1}

11.1.4 Synchronization with Data Field Sync

The start of the transmitter identifier pattern (i.e., the generation of the first bit of the serial code to be output from the shift register arrangement of Figure 11.1 following preloading) shall occur at such a time as to cause the BSS symbol corresponding thereto to be emitted simultaneously with the first symbol of the data segment sync of the first data segment following Data Field Sync or Data Frame Sync of the host 8-VSB signal. By virtue of the length of a complete sequence, the code sequence shall occur three and a fraction times within a Data Field and shall be truncated during the fourth sequence in a Data Field upon reaching the data segment sync at the start of the next Data Field Sync or Data Frame Sync data segment.

11.1.5 Future Enhancements

Development of the codes to be used for transmitter and network identification and station signaling may continue after adoption of this Standard. Designers of systems are advised to generate the transmitter and network identifier codes in programmable devices and to allow excess capacity for future growth of at least 50 percent more gates than are required to generate the code using the shift register scheme contained herein. Designers of systems are also advised that other truncation schemes might be adopted in the future; e.g., a method is possible in which each occurrence of the code sequence is truncated so that all four sequences within a data field are of equal length. Longer code sequences are also possible; e.g., a code sequence based upon shift registers of 18, 18, and 9 bits length would yield a code sequence slightly longer than a data field, requiring truncation of each sequence to make it fit within a data field.

11.2 Code Transmission

Transmission of the codes defined in Section 11.1 results in a signal at the bury ratio specified in Section 6.7.5. It produces an "RF watermark" signal having the features of 2-VSB transmission and the same emitted spectrum as the host 8-VSB signal.

11.2.1 2-VSB Signal

The buried spread spectrum (BSS) RF watermark signal shall be transmitted as a 2-VSB signal at an amplitude below the host 8-VSB signal as specified in Section 6.7.5. The characteristics of the 2-VSB signal, other than its amplitude and its framing structure, shall be identical to those of the Data Field Sync data segment as specified in A/53B Annex D.

11.2.2 Symbol Synchronization

The symbols of the BSS RF watermark signal shall be synchronized with those of the host 8-VSB signal so as to be emitted at the same times. There shall be no framing structure applied to the BSS code signal. The BSS code signals shall continue during the data segment sync symbols of the host 8-VSB signal. The BSS code signals shall not be transmitted during the Data Field Sync data segments. Upon arrival at the time designated for the next pre-load of the code pattern seed for a transmitter, the then current code sequence shall be truncated and the sequence started anew.

11.2.3 Emitted Spectrum

The emitted spectrum of the BSS RF watermark signal, taken by itself, shall conform to that depicted in Figures D3 and D12 of the ATSC A/53B standard, with the exception that the ratio between the amplitudes of the BSS RF watermark and of the pilot shall reflect the bury ratio in use for the RF watermark signal.

11.3 Modulation by Serial Data Stream

As described in Section 6.5.2, provision is made for inclusion of slow speed return channel data in the watermark signal. The return channel data is formatted as a start-stop code that is modulated onto the watermark signal. All modulation and signaling is synchronous with the data structure of the host 8-VSB signal.

11.3.1 Modulation of RF Watermark Signal

Modulation of the RF watermark signal shall be by phase inversion of the code sequence associated with a transmitter. The phase inversions shall occur on a data-field-by-data-field basis.

11.3.1.1 Phase Inversion of RF Watermark

Phase inversion modulation of the RF watermark signal shall occur through inversion on a bit-bit basis of the output of the code sequence generator shown in Figure 11.1. A non-inverted sequence shall represent a zero or space bit, and an inverted sequence shall represent a one or mark bit.

11.3.1.2 Bit-Synchronous with Data Fields

Inversions shall occur for complete data fields in the host 8-VSB data structure; i.e., synchronously with the preloading of the code sequence generator. Serial data stream bits thus have lengths of approximately 24.2 ms, and the resulting baud rate is about 41.3 baud.

11.3.2 Serial Data Stream

The serial data stream carried by the watermark signal shall be formatted using start-stop coding and shall carry ASCII data.

11.3.2.1 Start-Stop Code

The start-stop coding of the serial data stream shall use two start bits, one stop bit, seven data bits, and one even parity bit.

11.3.2.2 ASCII Data

The serial data stream shall use ASCII coding to represent the data bits for transmission. With parity coding in use, the 128-character ASCII data set shall be used.