(Proposed Standard) Annex D: RF/Transmission System Characteristics (Normative)

1. SCOPE

This Annex describes the characteristics of the RF/Transmission subsystem, which is referred to as the VSB subsystem, of the Digital Television Standard. The VSB subsystem offers two major modulation methods: a terrestrial broadcast method (8 VSB), and a high data rate method (16 VSB). These are described in separate sections of this document.

The 8-VSB modulation method is further defined by a set of required elements and various combinations of optional elements. The set of required elements is called the Main mode. Main service data is protected by the 'Main' Forward Error Correction (FEC) system and is sent using mandatory training sequences.

The optional enhancements add additional forward error correction coding layers to the data before sending the data via a constrained version of 8-VSB called Enhanced 8-VSB (E8-VSB). Various coding rate options are defined, and the payload assignment between the Enhanced 8-VSB and the Main Mode data is selectable at discretely defined values.

These Modes shall only be used in the defined combinations.

Accordingly, the 8 VSB transmission system offers optional sub-modes of operation that trade-off data rate for performance. The optional modes facilitate receiver operation in certain propagation conditions, with the degree of additional enhancements selected by the broadcaster with an acceptance of a reduction in the payload of the Main Service. The optional modes are designed to avoid impact on any remaining payload in the Main Service.

2. NORMATIVE REFERENCES

[D1] ISO/IEC IS 13818-1:1 2000 (E), International Standard: Information technology – Generic coding of moving pictures and associated audio information: systems.

3. COMPLIANCE NOTATION

As used in this document, "shall" denotes a mandatory provision of the standard. "Should" denotes a provision that is recommended but not mandatory. "May" denotes a feature whose presence does not preclude compliance that may or may not be present at the option of the implementer.

4. ABBREVIATIONS

FEC – Forward Error Correction

MPEG – Moving Pictures Experts Group

MUX – Multiplexer

PCR – Program Clock Reference

RS – Reed-Solomon (error correction coding)

VSB – Vestigial sideband modulation

5. TRANSMISSION CHARACTERISTICS FOR TERRESTRIAL BROADCAST

The terrestrial broadcast mode (known as 8 VSB) delivers an MPEG-2 Transport Stream (MPEG-2-TS) of up to 19.39 Mbps in a 6 MHz channel. Two optional modes use higher order data coding, called Enhanced 8-VSB. Enhanced data modes allow the broadcaster to allocate a portion of the base 19.39 Mbps data rate to Enhanced data transmission. Enhanced data is designed to have higher immunity to certain channel impairments than the Main Service but delivers data at a reduced information rate selected by the broadcaster from the specified options.

5.1 Overview of Main Service

See Figure D5. 1[1] for the functional block diagram of the Main Service alone. Incoming data is randomized and then processed for forward error correction (FEC) in the form of Reed-Solomon (RS) coding (20 RS parity bytes are added to each MPEG-2 packet), 1/6 data field interleaving and 2/3 rate trellis coding. The randomization and FEC processes are not applied to the sync byte of the transport packet, which is represented in transmission by a Data Segment Sync signal as described below. Following randomization and forward error correction processing, the data packets are formatted into Data Frames for transmission and Data Segment Sync and Data Field Sync are added.

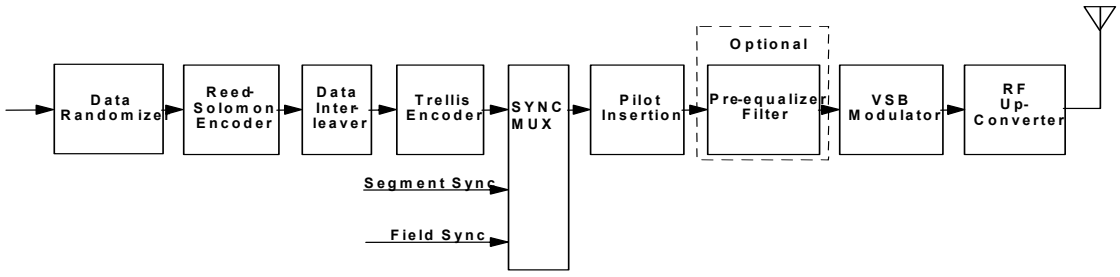


Figure D5.1 Main Service functional block diagram.

[1] Note that the optional pre-equalizer and RF Up-Converter blocks are implementation dependent and not addressed in this Annex.

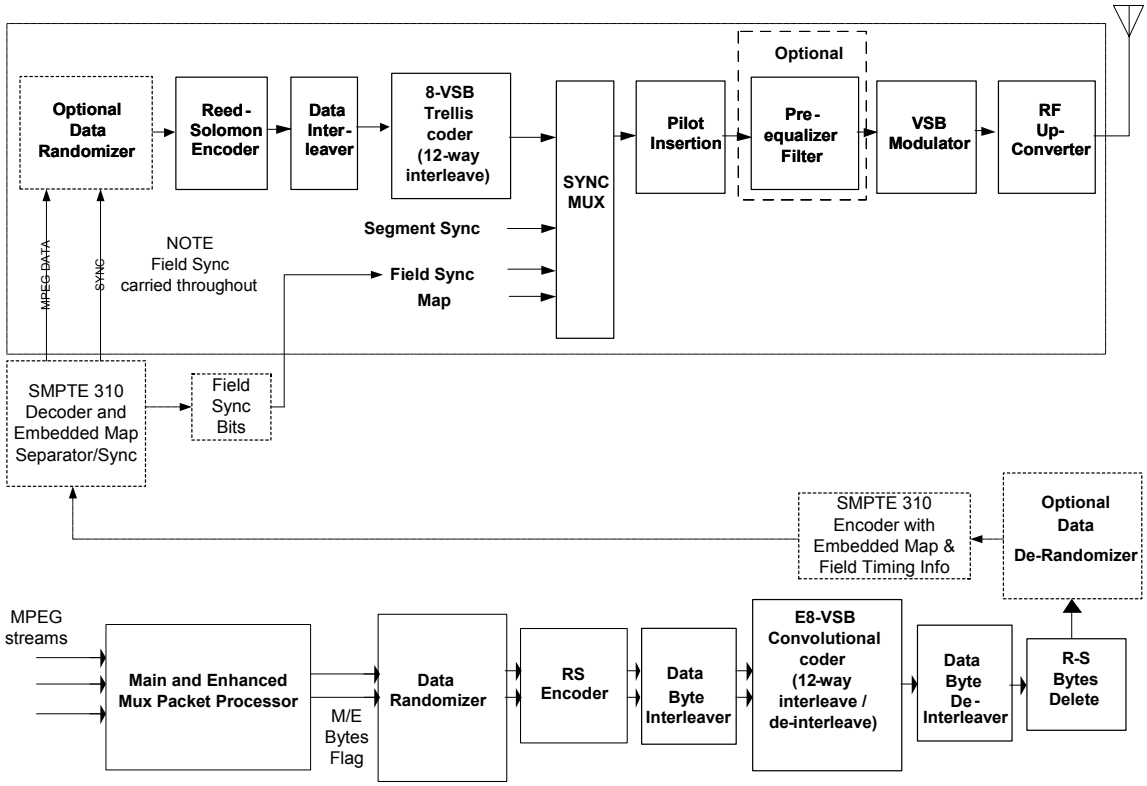


Figure D5.2 Main and Enhanced Service Functional Block Diagram

5.2 Overview of Main and Enhanced Service

See Figure D5.2 for Enhanced mode alternative functional block diagrams of the 8 VSB transmitter. Transmitting Enhanced 8-VSB (E8-VSB) requires processing as shown in Figure D5.2, Figure D5.10, Figure D5.11, Figure D5.12, and Figure D5.13. The upper row of Figure D5.2 consists of blocks that are common to the transmission of Enhanced streams (containing both Enhanced and Main data) and to the transmission of Main-only streams. The lower two rows contain blocks that are required for Enhanced transmission. Blocks in Figure D5.2 that are optional but that may be used to facilitate particular implementations will be called out in the following discussion.

MPEG-2 streams for Main and Enhanced processing are received at the input (lower left of Figure D5.2). Appropriate buffering for intra-data-field multiplexing is inserted on both the Main and the Enhanced MPEG-2 streams. Enhanced data is sent through the Main and Enhanced Mux Packet Processor as shown. Details of this block are given in Section 5.4.2 1 Figure D5.10, and Figure D5.11. Enhanced data shall be expanded by the ratio of 1:2 (for 1/2 rate coding) or 1:4 (for 1/4 rate coding) to form place-holder bits for the Enhanced convolutional coding and shall be formatted in MPEG-2 packets that shall be multiplexed with packets from the Main MPEG-2 stream. The order of multiplexing is determined according to the placement of Enhanced data segments in the transmitted data field (see Section 5.4.2.1.1 and 5.8 below).

All packets and an associated Main/Enhanced flag bit sequence (which indicates whether or not a specific byte is from a Main Service packet) shall pass through a data randomizer, RS

encoder, and byte interleaver that are identical to the ones used for Main-data-only transmission. The data shall then be processed by an E8-VSB convolutional trellis coder, which shall have two modes of operation for the Enhanced and Main data respectively, controlled by the Main/Enhanced (M/E) flag.

The Enhanced convolutional processing, as specified below, shall result in replacement of the placeholder bits in the expanded Enhanced stream packets (including the additional RS FEC data). The symbols at the output of the E8-VSB convolutional coder shall be de-interleaved at the 12:1 trellis level and then at the byte level. The output of this stage is groups of bytes with appended erroneous RS coded parity bytes, due to changes in the symbol data produced by the E8-VSB convolutional trellis coder. The erroneous RS coded parity bytes shall be deleted and replaced by correct bytes generated by the following RS encoder (top row of Figure D5.2). A data de-randomizer /randomizer pair may be inserted at this point to reformulate packets that are transmitted by a SMPTE 310 link.

In case the upper and lower rows of processing in Figure D5.2 are physically separated (as by a SMPTE 310 link), means will be required to transmit the map data and the field sync timing across that link from the multiplexer (lower left of Figure D5.2) to the insertion mux (upper row of Figure D5.2). Such methods are discussed in other ATSC standards. If the SMPTE 310 link is used, then the embedded map and synchronization information is decoded and is sent to the 8-VSB transmitter shown in the upper row. Data to signal the placement of Enhanced data segments within the data field ("map data") shall be transmitted during the data field sync segment, as described below (see Section 5.7).

5.3 Data Organization

Figure D5.3 shows how the data are organized for transmission. Each Data Frame consists of two Data Fields, each containing 313 Data Segments. The first Data Segment of each Data Field is a unique synchronizing signal (Data Field Sync) and includes the training sequence used by the equalizer in the receiver. The remaining 312 Data Segments each carry the equivalent of the data from one 188-byte transport packet plus its associated RS-FEC overhead. The actual data in each Data Segment comes from several transport packets because of data interleaving. In the case of E8-VSB transmission, the Enhanced-coded 8-level symbols are dispersed among the normal 8-level symbols due to additional interleaving of Enhanced coding. Each Data Segment consists of 832 symbols. The first 4 symbols are transmitted in binary form and provide segment synchronization. This Data Segment Sync signal also represents the sync byte of the 188-byte MPEG-2-compatible transport packet[2]. The remaining 828 symbols of each Data Segment carry data equivalent to the remaining 187 bytes of a transport packet and its associated RS-FEC overhead. These 828 symbols are transmitted as 8-level signals and therefore carry three bits per symbol. Thus, 828 x 3 = 2484 bits of data are carried in each Data Segment, which exactly matches the requirement to send a protected transport packet:

187 data bytes + 20 RS parity bytes = 207 bytes

207 bytes x 8 bits/byte = 1656 bits

[2] Note that E8-VSB data includes additional RS coding and additional trellis coding. The packet expansion by a ratio of 1:2 or 1:4 for Rate 1/2 or 1/4 respectively. Due to this expansion, an MPEG-2 packet that is input to the enhanced stream extends over a non-integral multiple of normal segments before being dispersed by interleaving. The Data Segment Sync is MPEG-2 sync byte of the enhanced payload.

2/3 rate trellis coding requires 3/2 x 1656 bits = 2484 bits.

The exact symbol rate is given by Equation 1 below:

(1) S_r (MHz) = 4.5/286 x 684 = 10.76... MHz

The frequency of a Data Segment is given in Equation 2 below:

(2) fseg= S_r / 832 = 12.94... X 10^3 Data Segments/s.

The Data Frame rate is given by Equation (3) below:

(3) $f_{frame} = f_{seg}/626$ = 20.66 ... frames/s.

The symbol rate S_r and the transport rate T_r (see Section 7.2 of Annex C) shall be locked to each other in frequency.

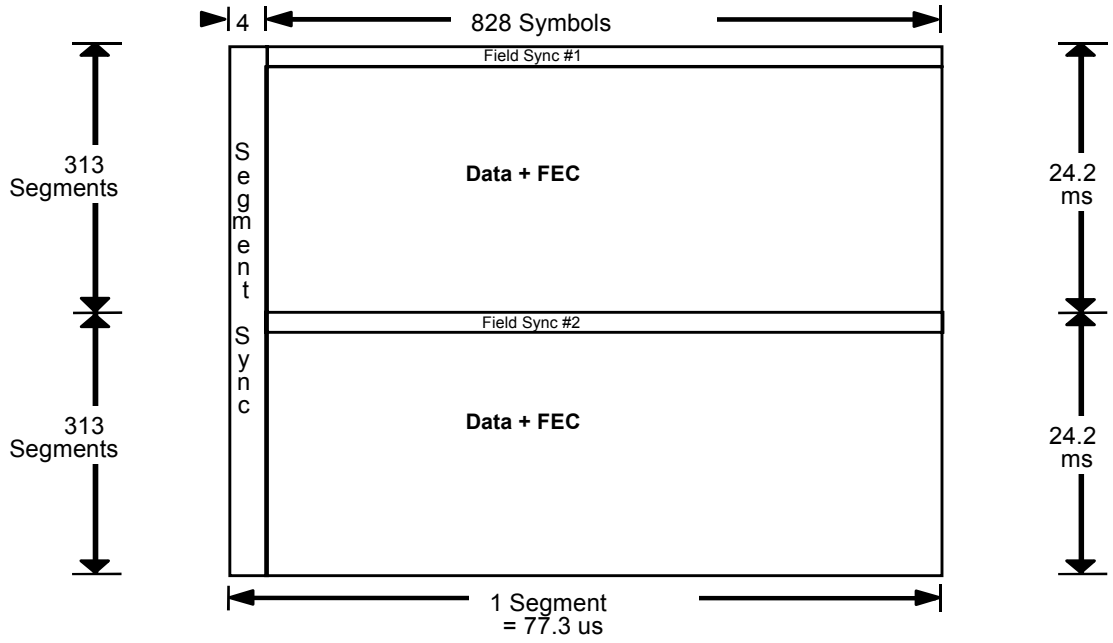


Figure D5.3 VSB data frame without extra field sync.

The 8-level symbols combined with the binary Data Segment Sync and Data Field Sync signals shall be used to suppressed-carrier modulate a single carrier. Before transmission, however, most of the lower sideband shall be removed. The resulting spectrum is flat, except for the band edges where a nominal square root raised cosine response results in 620 kHz transition regions. The nominal VSB transmission spectrum is shown in Figure D5.4.

At the suppressed-carrier frequency, 310 kHz from the nominal lower band edge, a small pilot shall be added to the signal.

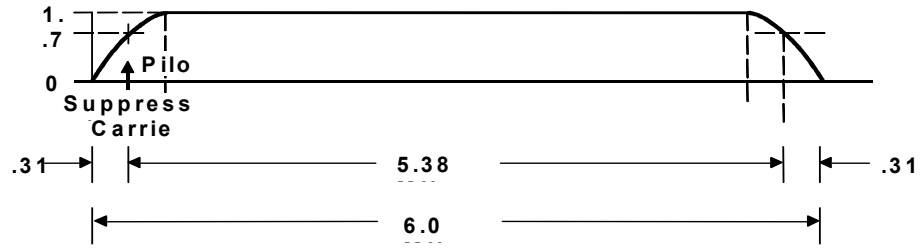


Figure D5.4 VSB channel occupancy (nominal)

5.4 Channel Error Protection

Main channel error protection consists of a concatenated RS encoding, interleaving and 4-state trellis encoding for the Main Service.

As an option, Enhanced modes may be employed. There are two modes available, with choice of levels of error protection within each method defined. These Enhanced modes provide methods to trade off data rate from the Main Service to facilitate reception. For a particular mode choice, the data rate assigned to the mode is variable in pre-defined steps.

There is a set of methods for adding additional forward error correction coding layers to the data before sending the data via a constrained version of 8-VSB. This method is called Enhanced 8-VSB. Various coding rate options are defined, and the payload assignment between the Enhanced 8-VSB data and the Main data is selectable at defined values.

The Main Service channel error protection is specified first, followed by the Enhanced mode.

5.4.1 Main Service Data Error Detection and Correction Facility

5.4.1.1 Main Service Data Randomizer

A data randomizer shall be used on all input data (including an Enhanced stream if present) to randomize the data payload. The data randomizer XORs all the incoming data bytes with a 16-bit maximum length pseudo random binary sequence (PRBS) which is initialized at the beginning of the Data Field. The PRBS is generated in a 16-bit shift register that has 9 feedback taps. Eight of the shift register outputs are selected as the fixed randomizing byte, where each bit from this byte is used to individually XOR the corresponding input data bit. The data bits are XORed MSB to MSB ... LSB to LSB.

The randomizer generator polynomial is as follows:

$$G_{(16)} = X^{16} + X^{13} + X^{12} + X^{11} + X^{7} + X^{6} + X^{3} + X + 1$$

The initialization (pre-load) to F180 hex (load to 1) occurs during the Data Segment Sync interval prior to the first Data Segment.

The randomizer generator polynomial and initialization is shown in Figure D5.5.

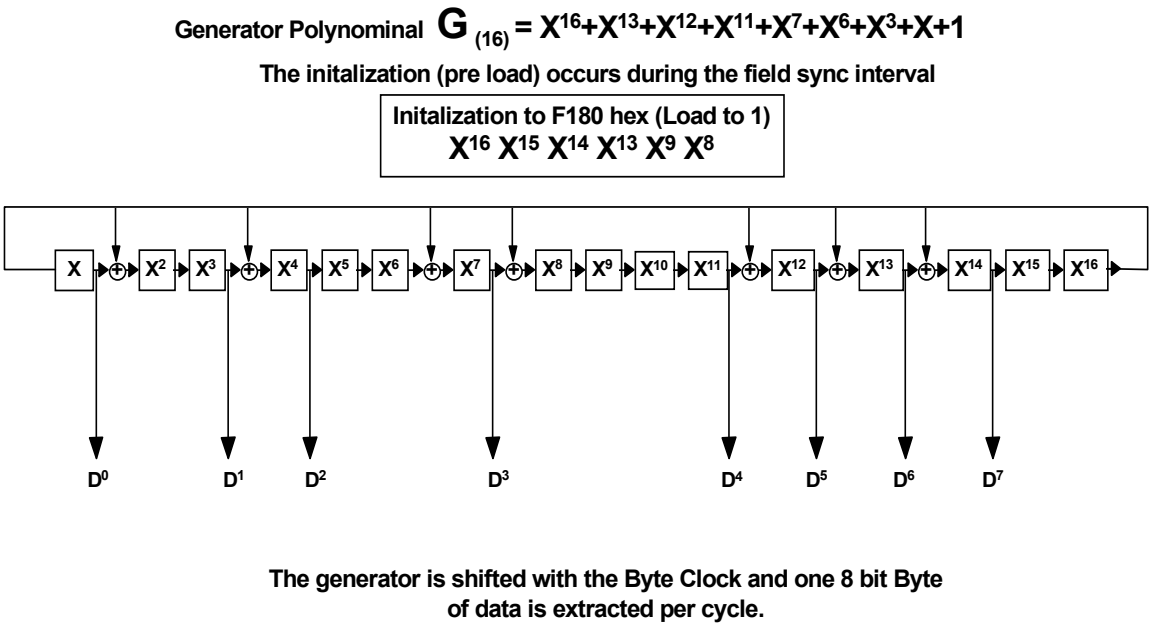


Figure D5.5 Randomizer polynomial.

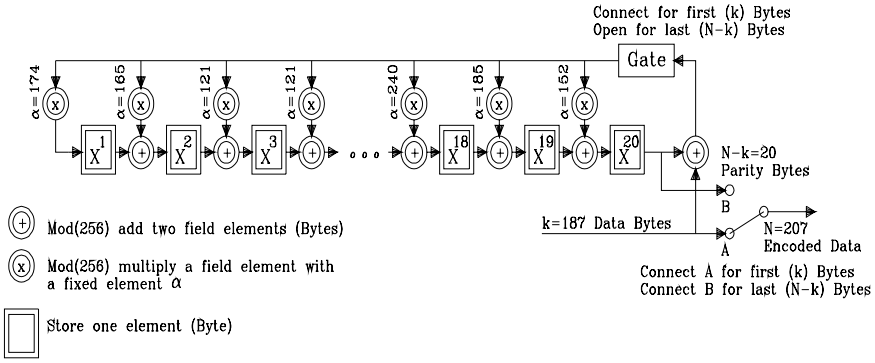
5.4.1.2 Main Service Reed-Solomon Encoder

The randomizer output is the input for the RS Encoder. The RS code used in the VSB transmission subsystem shall be a t = l0 (207,187) code. The RS data block size is 187 bytes, with 20 RS parity bytes added for error correction. A total RS block size of 207 bytes is transmitted per Data Segment.

In creating bytes from the serial bit stream, the MSB shall be the first serial bit. The 20 RS parity bytes shall be sent at the end of the Data Segment. The parity generator polynomial and the primitive field generator polynomial are shown in Figure D5.6.

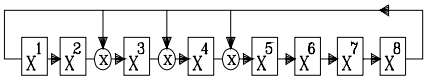
$$\prod_{i=0}^{i=2t-1}(X+\alpha^{i}) = X^{20} + X^{19}\alpha^{17} + X^{18}\alpha^{60} + X^{17}\alpha^{79} + X^{16}\alpha^{50} + X^{15}\alpha^{61} + X^{14}\alpha^{163} + X^{13}\alpha^{26} + X^{12}\alpha^{187} + X^{11}\alpha^{202} + X^{10}\alpha^{180} + X^{9}\alpha^{221} + X^{8}\alpha^{225} + X^{7}\alpha^{83} + X^{6}\alpha^{239} + X^{5}\alpha^{156} + X^{4}\alpha^{164} + X^{3}\alpha^{212} + X^{2}\alpha^{212} + X^{1}\alpha^{188} + \alpha^{190}$$

$$= X^{20} + 152X^{19} + 185X^{18} + 240X^{17} + 5X^{16} + 111X^{15} + 99X^{14} + 6X^{13} + 220X^{12} + 112X^{11} + 150X^{10} + 69X^{9} + 36X^{8} + 187X^{7} + 22X^{6} + 228X^{5} + 198X^{4} + 121X^{3} + 121X^{2} + 165X^{1} + 174$$



Primitive Field Generator Polynomial (Galois Field)

$$G(256) = X^{8} + X^{4} + X^{3} + X^{2} + 1$$



Each shift of the generator produces a field element

Figure D5.6 Reed-Solomon (207,187) t=10 parity generator polynomial.

5.4.1.3 Main Service Interleaving

The interleaver employed in the VSB transmission system shall be a 52 data segment (intersegment) convolutional byte interleaver. Interleaving is provided to a depth of about 1/6 of a data field (4 ms deep). Only data bytes (including the RS parity bytes) shall be interleaved. The interleaver shall be synchronized to the first data byte of the data field. Intrasegment interleaving is also performed for the benefit of the trellis coding process. The convolutional interleaver is shown in Figure D5.7.

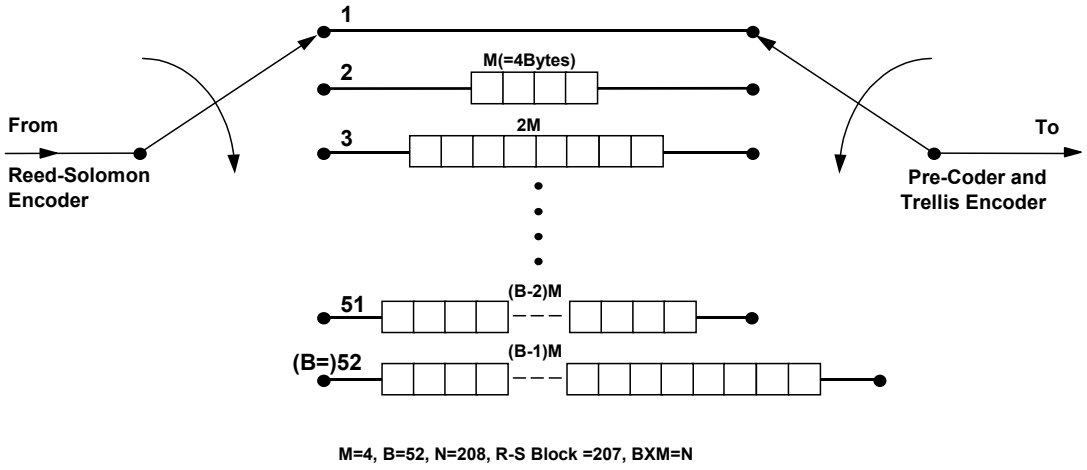


Figure D5.7 Convolutional interleaver (byte shift register illustration).

5.4.1.4 Main Service Trellis Coding

The 8 VSB transmission sub-system shall employ a 2/3 rate (R=2/3) trellis code (with one unencoded bit which is precoded). That is, one input bit is encoded into two output bits using a l/2 rate convolutional code while the other input bit is precoded. The signaling waveform used with the trellis code is an 8-level (3 bit) one-dimensional constellation. The transmitted signal is referred to as 8 VSB. A 4-state trellis encoder shall be used.

Trellis code intrasegment interleaving shall be used. This uses twelve identical trellis encoders and precoders operating on interleaved data symbols. The code interleaving is accomplished by encoding symbols (0, 12, 24, 36 ...) as one group, symbols (1, 13, 25, 37, ...) as a second group, symbols (2, 14, 26, 38, ...) as a third group, and so on for a total of 12 groups.

In creating serial bits from parallel bytes, the MSB shall be sent out first: (7, 6, 5, 4, 3, 2, 1, 0). The MSB is precoded (7, 5, 3, 1) and the LSB is feedback convolutional encoded (6, 4, 2, 0). Standard 4-state optimal Ungerboeck codes shall be used for the encoding. The trellis code utilizes the 4-state feedback encoder shown in Figure D5.8. Also shown is the precoder and the symbol mapper. The trellis code and precoder intrasegment interleaver is shown in Figure D5.9 which feeds the mapper detailed in Figure D5.8. Referring to Figure D5.9, data bytes are fed from the byte interleaver to the trellis coder and precoder, and they are processed as whole bytes by each of the twelve encoders. Each byte produces four symbols from a single encoder.

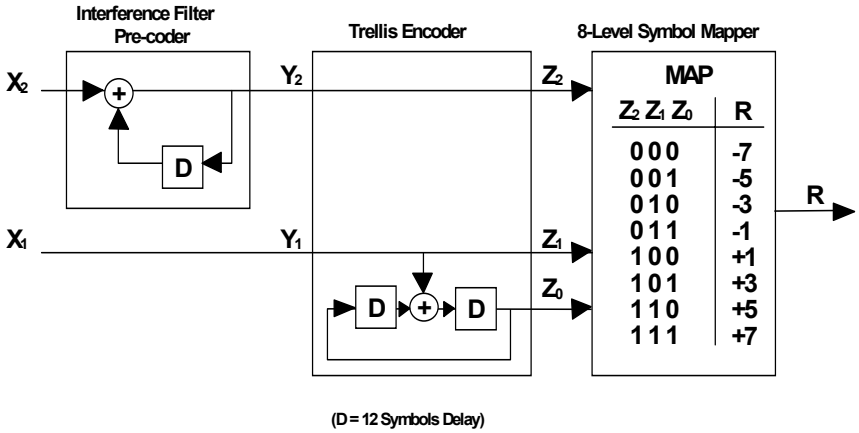


Figure D5.8 Main Service trellis encoder, precoder, and symbol mapper.

The output multiplexer shown (as the right circle) in Figure D5.9 shall advance by four symbols on each segment boundary. However, the state of the trellis encoder shall not be advanced. The data coming out of the multiplexer shall follow normal ordering from encoder 0 through 11 for the first segment of the frame, but on the second segment the order changes and symbols are read from encoders 4 through 11, and then 0 through 3. The third segment reads from encoder 8 through 11 and then 0 through 7. This three-segment pattern shall repeat through the 312 Data Segments of the frame. Table D5.1 shows the interleaving sequence for the first three Data Segments of the frame.

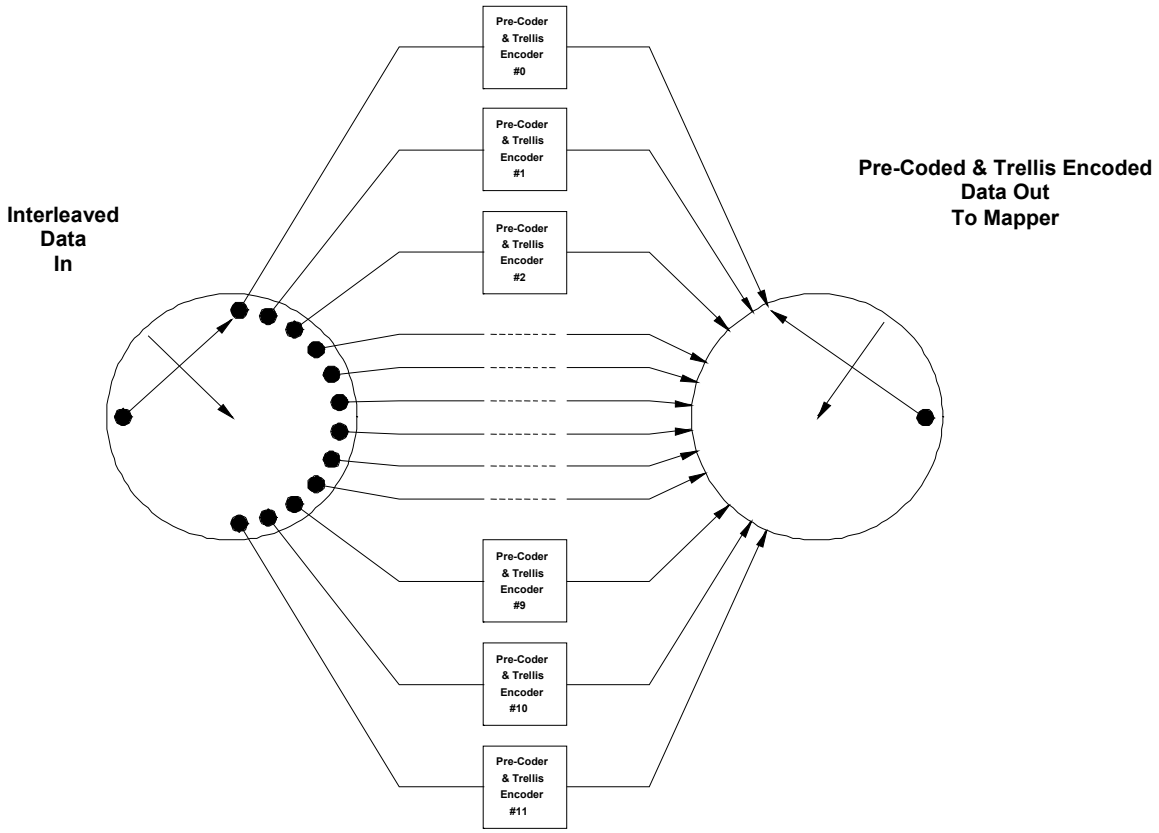


Figure D5.9 Trellis code interleaver.

After the Data Segment Sync is inserted, the ordering of the data symbols is such that symbols from each encoder occur at a spacing of twelve symbols.

Table D5.1 Interleaving Sequence

Segment	Block 0	Block 1	...	Block 68
0	D0 D1 D2 ... D11	D0 D1 D2 ... D11	...	D0 D1 D2 ... D11
1	D4 D5 D6 ... D3	D4 D5 D6 ... D3	...	D4 D5 D6 ... D3
2	D8 D9 D10 ... D7	D8 D9 D10 ... D7	...	D8 D9 D10 ... D7

A complete conversion of parallel bytes to serial bits needs 828 bytes to produce 6624 bits. Data symbols are created from 2 bits sent in MSB order, so a complete conversion operation yields 3312 data symbols, which corresponds to 4 segments of 828 data symbols. 3312 data symbols divided by 12 trellis encoders gives 276 symbols per trellis encoder. 276 symbols divided by 4 symbols per byte gives 69 bytes per trellis encoder.

The conversion starts with the first segment of the field and proceeds with groups of 4 segments until the end of the field. 312 segments per field divided by 4 gives 78 conversion operations per field.

Allowing for segment sync the input to 4 encoders is skipped but the encoders cycle with no input. The input is held until the next multiplex cycle and then fed to the correct encoder.

Table D5.2 details the byte to symbol conversion and the associated multiplexing of the trellis encoders. Segment 0 is the first segment of the field. The pattern repeats every 12 segments; segments 5 through 11 are not shown.

Table D5.2 Byte to Symbol Conversion, Multiplexing of Trellis Encoders

Symbol	Segment 0			Segment 1			Segment 2			Segment 3			Segment 4		
	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits
0	0	0	7,6	4	208	5,4	8	412	3,2	0	616	1,0	4	828	7,6
1	1	1	7,6	5	209	5,4	9	413	3,2	1	617	1,0	5	829	7,6
2	2	2	7,6	6	210	5,4	10	414	3,2	2	618	1,0	6	830	7,6
3	3	3	7,6	7	211	5,4	11	415	3,2	3	619	1,0	...	...	...
4	4	4	7,6	8	212	5,4	0	416	3,2	4	620	1,0	...	...	...
5	5	5	7,6	9	213	5,4	1	417	3,2	5	621	1,0	...	...	...
6	6	6	7,6	10	214	5,4	2	418	3,2	6	622	1,0	...	...	...
7	7	7	7,6	11	215	5,4	3	419	3,2	7	623	1,0	...	...	...
8	8	8	7,6	0	204	5,4	4	408	3,2	8	612	1,0	...	...	...
9	9	9	7,6	1	205	5,4	5	409	3,2	9	613	1,0	...	...	...
10	10	10	7,6	2	206	5,4	6	410	3,2	10	614	1,0	...	...	...
11	11	11	7,6	3	207	5,4	7	411	3,2	11	615	1,0	...	...	...
12	0	0	5,4	4	208	3,2	8	412	1,0	0	624	7,6	...	...	...
13	1	1	5,4	5	209	3,2	9	413	1,0	1	625	7,6	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
19	7	7	5,4	11	215	3,2	3	419	1,0	7	631	7,6	...	...	...
20	8	8	5,4	0	204	3,2	4	408	1,0	8	632	7,6	...	...	...
21	9	9	5,4	1	205	3,2	5	409	1,0	9	633	7,6	...	...	...
22	10	10	5,4	2	206	3,2	6	410	1,0	10	634	7,6	...	...	...
23	11	11	5,4	3	207	3,2	7	411	1,0	11	635	7,6	...	...	...
24	0	0	3,2	4	208	1,0	8	420	7,6	0	624	5,4	...	...	...
25	1	1	3,2	5	209	1,0	9	421	7,6	1	625	5,4	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
31	7	7	3,2	11	215	1,0	3	427	7,6	...	...	...	...	...	...
32	8	8	3,2	0	204	1,0	4	428	7,6	...	...	...	...	...	...
33	9	9	3,2	1	205	1,0	5	429	7,6	...	...	...	...	...	...
34	10	10	3,2	2	206	1,0	6	430	7,6	...	...	...	...	...	...
35	11	11	3,2	3	207	1,0	7	431	7,6	...	...	...	...	...	...
36	0	0	1,0	4	216	7,6	8	420	5,4	...	...	...	...	...	...
37	1	1	1,0	5	217	7,6	9	421	5,4	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
47	11	11	1,0	3	227	7,6	...	...	...	...	...	...	...	...	...
48	0	12	7,6	4	216	5,4	...	...	...	...	...	...	...	...	...
49	1	13	7,6	5	217	5,4	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
95	11	23	1,0	...	...	...	...	...	...	...	...	...	...	...	...
96	0	24	7,6	...	...	...	...	...	...	...	...	...	...	...	...
97	1	25	7,6	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
767	11	191	1,0	...	...	...	...	...	...	...	...	...	...	...	...
768	0	192	7,6	...	...	...	...	...	...	...	...	...	...	...	...
769	1	193	7,6	...	...	...	...	...	...	...	...	...	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...

Symbol	Segment 0			Segment 1			Segment 2			Segment 3			Segment 4		
	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits	Trellis	Byte	Bits
815	11	203	1,0	3	419	7,6	7	623	5,4	11	827	3,2	...	...	...
816	0	204	7,6	4	408	5,4	8	612	3,2	0	816	1,0	...	...	...
817	1	205	7,6	5	409	5,4	9	613	3,2	1	817	1,0	...	...	...
...	...	...	...	...	...	...	...	...	...	...	...	...	...	...	...
827	11	215	7,6	3	419	5,4	7	623	3,2	11	827	1,0	...	...	...

5.4.2 Main and Enhanced Service Data Error Detection and Correction Facilities

When Enhanced Services are enabled (see Figure D5.2), the processing steps for both Main Service data and Enhanced Service data are somewhat different than for Main Service data alone. The requirements for the RF transmission system with Enhanced data capability are specified hereinunder.

5.4.2.1 Enhanced Data Protection

Enhanced data is protected by a concatenated FEC comprised by an additional FEC (applied to the Enhanced Service) and by the Main FEC. Enhanced channel error protection uses an additional interleaver (Enhanced interleaver), an additional Reed Solomon encoding scheme (Enhanced RS encoding), an additional convolutional interleaver (Enhanced convolutional interleaver), and an additional 4-state convolutional encoder (Enhanced convolutional encoder). The Enhanced data and Enhanced RS parity bytes are encapsulated within the transport level payload portion of an MPEG-2 Packet. The Enhanced 4-state convolutional encoder is concatenated and synchronized with the Main trellis 4-state encoding to produce an effective 16-state trellis encoder for the Enhanced data. Enhanced FEC offers two encoding modes defined as 1/2 rate and 1/4 rate E8-VSB modes. The following sections establish requirements for each functional block of the Enhanced FEC shown in Figure D5. 2 Main and Enhanced Mux Packet Processor.

The input to the preprocessor shall be 188-byte MPEG-2 packets.

The data intended to be encoded by the Main and Enhanced FEC is split into a maximum of three parallel streams. Each stream is associated with a Main, an Enhanced 1/2 rate, or an Enhanced 1/4 rate FEC mode status.

Appropriate buffering is inserted in both the Main and the Enhanced MPEG-2 streams, and Enhanced data is sent through the E8-VSB Pre-Processor. Enhanced data shall be Reed Solomon encoded, and each byte shall be expanded by the ratio of 1:2 (for 1/2 rate coding) or 1:4 (for 1/4 rate coding) to form place-holder bits for the 4-state Enhanced convolutional coding. The expanded bytes shall be formatted in MPEG-2 compliant packets, which shall be multiplexed with packets from the Main MPEG-2 stream (Main Service).

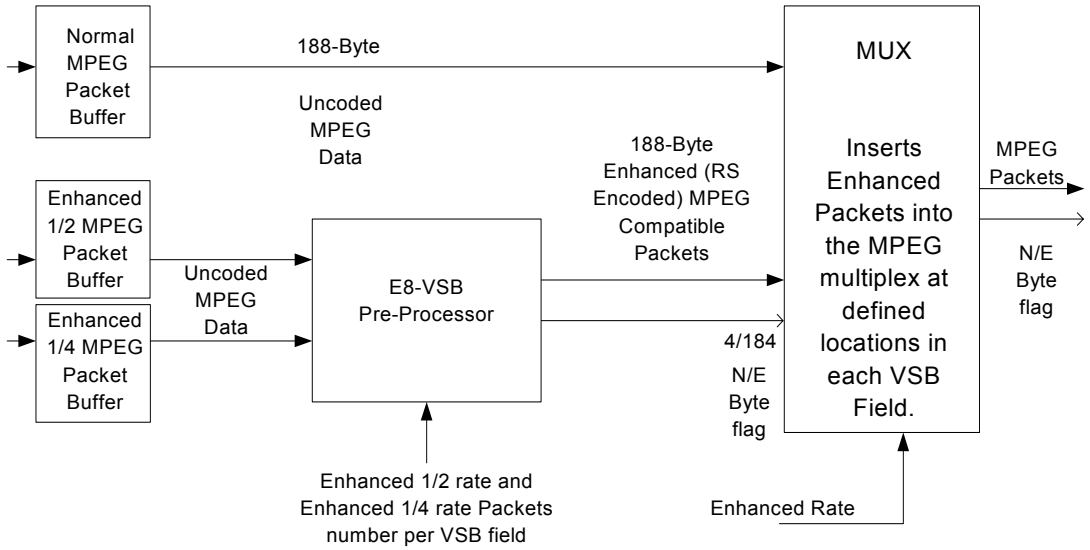


Figure D5.10 Main and Enhanced Mux Packet Processor.

5.4.2.1.1 E8-VSB pre-processor

5.4.2.1.1.1 164-byte packet converter

The data intended to be encoded with either the 1/2 rate Enhanced FEC or the 1/4 rate Enhanced FEC shall be processed by the packet converter, which shall organize the 188-byte MPEG-2 data input into 164-byte packets.

5.4.2.1.1.2 Enhanced 1/2 rate and 1/4 rate packet Multiplexer

The payload of the Enhanced data, comprised of 1/2 rate and 1/4 rate 164-byte packets to be transmitted in a VSB field, is specified by the E-VSB map and is constant for a group of sixteen VSB frames (see Section 5.7).

The 1/2 rate and 1/4 rate 164-byte packets corresponding to the Enhanced payload carried by a VSB frame are packed in a buffer prior to being sent to the RS encoder. The maximum number of 164-byte packets allowed for the Enhanced 1/2 rate mode is 156. The maximum number of 164-byte packets allowed for the Enhanced 1/4 rate mode is 78. The maximum buffer depth shall be 156.

Placement of the 1/2 rate and 1/4 rate 164-byte packets shall occur at specific locations in the multiplexing buffer. The location of the Enhanced 164-byte packet in the Enhanced multiplexer buffer shall be defined as follows:

- When the 10th bit of the 12-bit payload of the E-VSB map (starting from the leftmost bit) is set to '1', the 164-byte packets will alternate between 1/2 rate and 1/4 rate packets until the number of Enhanced 164-byte packets intended to be carried by the 8-VSB field is reached. The first Enhanced packet processed by the RS encoder shall be the first 1/2 rate packet (if 1/2 rate packets are present) incoming to the buffer multiplexer.
- When the 10th bit is set to 0, the 1/2 rate and the 1/4 rate 164-byte packets shall be grouped together. The buffer shall be segmented into two parts. The first part of the buffer shall contain, consecutively, all of the 1/2 rate 164-byte packets, and the second

part of the buffer shall contain, consecutively, all of the 1/4 rate 164-byte packets. The first packet processed by the RS encoder shall be the first 1/2 rate packet (if 1/2 rate packets are present) incoming to the buffer multiplexer.

Each PCR [D1] shall be adjusted to accommodate the actual MPEG-2 Transport Stream packet [D1] delivery time.

Additionally, the Enhanced multiplexer buffer shall carry an H/Q flag, which shall identify the nature of each 164-byte packet. This H/Q flag shall have two states: "H" for 1/2 rate and "Q" for 1/4 rate.

5.4.2.1.1.3 Enhanced RS

The first function after the segment multiplexer shall be an encoding of the 164-byte packets of data to be sent via this enhanced means by an RS encoder with parameters t = 10 (184,164). The Primitive Field Generating Polynomial shall be the same as that specified in Figure D5.6, which is also used for the Main RS encoder. The RS encoder will pass through the H/Q flag generated by the previous block and shall extend it to the parity bytes generated by the RS encoder.

5.4.2.1.1.4 Enhanced data interleaver

The interleaver is mainly intended to provide additional protection against burst noise and bursty errors produced by channel degradations. The Enhanced RS encoder shall be followed by an Enhanced data interleaver that shall perform a convolutional byte interleave with parameters B=46, M=4, N=184. The Enhanced interleaver shall make multiple complete revolutions per data field for all Enhanced data code rates. It shall start at the top (zero delay) row in the same manner as the Main byte interleaver. The interleaver for all mix percentages of Enhanced data shall introduce a constant delay to an MPEG-2 transport stream. The conceptual structure may be seen in Figure D5.7. The data interleaver shall carry the H/Q flag generated during the operation of buffer multiplexing of the 164-byte packets. The H/Q flag shall remain in time synchronization with each byte it describes.

5.4.2.1.1.5 Enhanced bytes expansion and addition of MPEG-2 header

Each byte associated with the Enhanced 1/2 rate FEC mode is expanded into two bytes. The expansion of the 1/2 rate byte is as specified below.

Original Enhanced Byte	Expanded Enhanced Byte (E7,E6,E5,E4,E3,E2,E1,E0)	Expanded Byte Number
(R7,R6,R5,R4,R3,R2,R1,R0)	(R7,X,R6,X,R5,X,R4,X)	1
	(R3,X,R2,X,R1,X,R0,X)	0

Each byte associated with the Enhanced 1/4 rate FEC mode is expanded into four bytes. The expansion of the 1/4 rate byte is as specified below.

Original Enhanced Byte	Expanded Enhanced Byte (E7,E6,E5,E4,E3,E2,E1,E0)	Expanded Byte Number
(R7,R6,R5,R4,R3,R2,R1,R0)	(R7,X,R7,X,R6,X,R6,X)	3
	(R5,X,R5,X,R4,X,R4,X)	2
	(R3,X,R3,X,R2,X,R2,X)	1
	(R1,X,R1,X,R0,X,R0,X)	0

The bits R7 through R0 of the original 1/2 rate and 1/4 rate bytes are respectively mapped into two and four Enhanced bytes. The bits E7 through E0 are bit positions in the subsequently expanded byte. The "X" in the expanded bytes denotes a placeholder and may be coded by 0.

For the rate 1/2, the expanded byte number "0" shall represent the LSB byte and the byte number "1" shall represent the MSB byte. For the rate 1/4, the expanded byte number "0" shall represent the LSB byte of the 4 bytes word, and the expanded byte number "3" shall represent the MSB byte. For both the 1/2 rate and 1/4 rate the original byte replacement shall start with the MSB byte of respectively the two and four expanded bytes.

The expanded bytes are formatted into 184-byte segments. Each reconstructed 184-byte segment packet may consist of both 1/2 rate and 1/4 rate expanded Enhanced bytes.

For the purpose of maintaining strict backward compatibility for existing receivers, a 0x47 Sync byte and the 3 MPEG-2 header bytes of each Main packet carrying Enhanced encoded data are mapped into the null packet designated by 0x1FFF and are prepended to each 184-byte Enhanced segment.

The encapsulated Enhanced RS encoding (184,164) in the E8-VSB Pre-Processor reduces the effective payload of these packets by an additional 20 bytes to 164.

After the introduction of the header bytes, the H/Q flag carried through the previous blocks is dropped. Another flag, called the M/E flag, is used and shall be in the Enhanced state when Enhanced bytes are clocked out of the E8-VSB Pre-Processor and shall be in the Main state when the 4-byte MPEG-2 header is clocked out of the E8-VSB Pre-Processor.

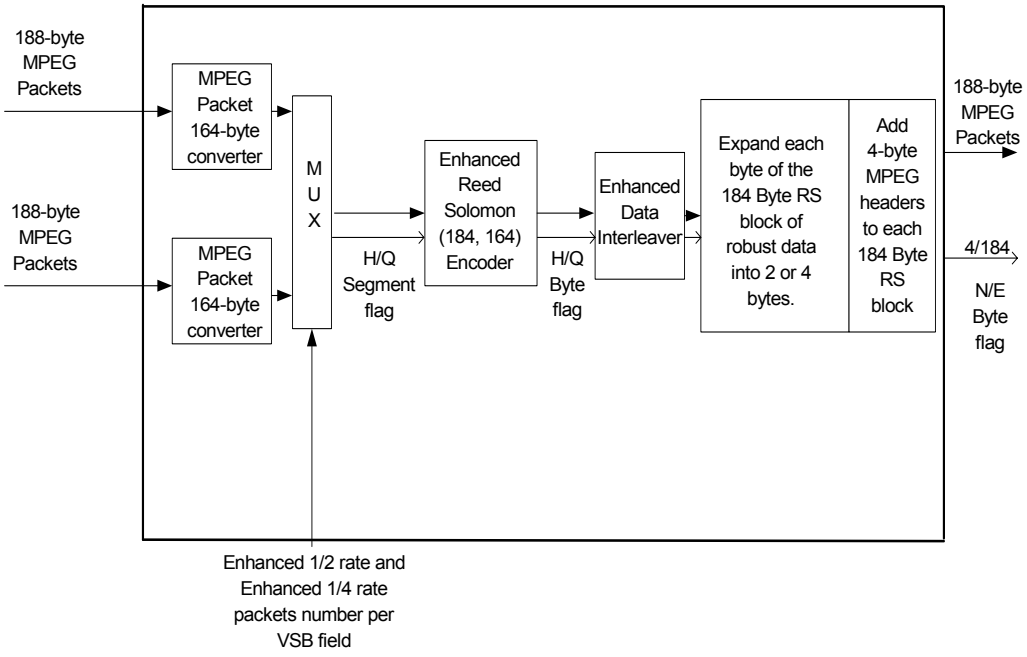


Figure D5.11 E8-VSB Pre-Processor.

5.4.2.2 Data Randomizer

The data byte processing shall be per Section 5.4.1.1, and the M/E flag shall not be modified and shall remain in time synchronization with each byte it describes. The value shall change state on byte boundaries when the associated byte belongs to a different class of bytes. The M/E flag shall be in the Main state when the bytes correspond to either the Main MPEG-2 packets or to the 4-byte header of the Enhanced MPEG-2 compliant packets. The M/E flag shall be in the Enhanced state when the bytes correspond to the payload of the reconstructed Enhanced MPEG-2 packets.

5.4.2.3 Reed Solomon Encoder

All bytes output from the data randomizer shall be sent to the RS encoder. The data byte processing shall be as specified in Section5.4.1.2, and the M/E flag shall be maintained as Enhanced for the 184 Enhanced bytes and shall be set to Main for all other bytes. All RS parity bytes are Main mode bytes and shall have their flags associated to their Main states.

5.4.2.4 Data Interleaver

The output of the Reed-Solomon Encoder, including both Main Service data and robust data, shall be interleaved by a convolutional data byte interleaver. This data interleaver shall have the same parameters as a Main-Service-only interleaver, as specified in Section 5.4.1.3. In addition, the Main/Enhanced (M/E) control signal from the Reed-Solomon Encoder (which changes state on byte boundaries) shall be interleaved using the same parameters as the data, so that the output M/E control signal shall correctly indicate the M/E type of each data byte output from the interleaver.

5.4.2.5 E8-VSB Convolutional Coder

The E8-VSB convolutional coder is comprised of a symbol interleaver, an Enhanced symbol processor, and a symbol de-interleaver. The symbol interleaver corresponds to the 12-way Trellis code interleaving described in Section 5.4.1.4. The M/E flag shall also go through the same interleaving as the symbol interleaver. The symbol de-interleaver shall be the inverse of the earlier described symbol interleaver, with the exception of the M/E flag, which is not passed through.

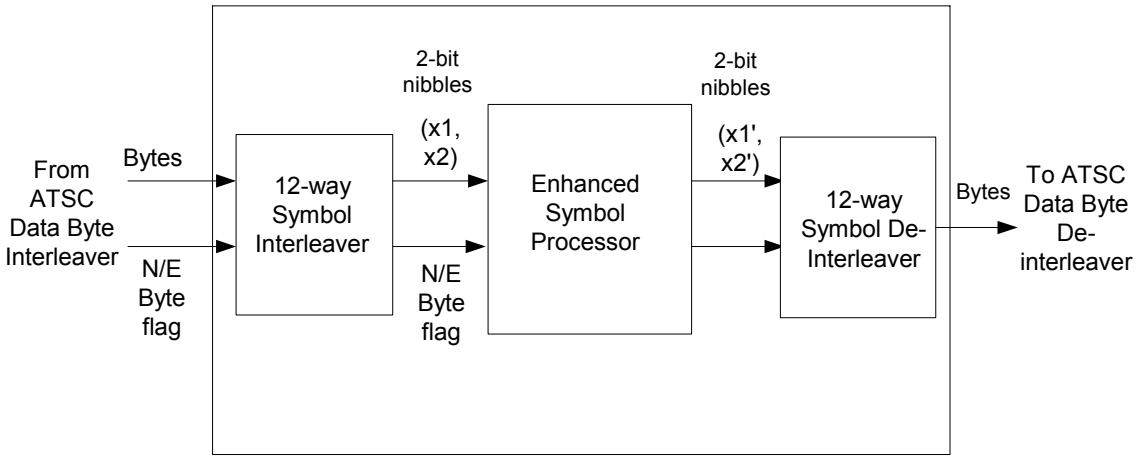


Figure D5.12 E8-VSB convolutional coder (12-way interleave/de-interleave).

5.4.2.5.1 Enhanced Symbol Processor

For reference, in the Main transmission mode, each of the 12 parallel trellis encoders receive and encode a byte of data from the Main interleaver in the following order: (7,6,5,4,3,2,1,0), where 7 is the MSB and 0 is the LSB.

The Enhanced symbol Processor contains the convolutional encoder with a 4-state feedback. The convolutional encoder process the incoming bytes by group of 2-bit nibbles. The convolutional code is the same as that for the normal trellis encoder, as illustrated in Figure D5.9. Referring to Figure D5.13, for all Enhanced transmission modes, the M/E flag selects the Enhanced input ("E") to the illustrated lower three muxes to perform convolutional encoding of the X2 bit to produce the X2' bit. For the Main mode of transmission, the control line selects the Main input ("N") of the muxes to hold the convolutional encoder in its current state and to derive the X1' bit directly from the X1 bit.

For normal bytes the four groups of 2-bit nibbles associated with one of the 12-convolutional encoders are passed through, and the states of the encoder are updated. For Enhanced bytes, bits in positions E7, E5, E3, and E1 are encoded by the systematic convolutional encoder. Bits in positions E6, E4, E2, and E0 are not processed. Placeholder of the four groups of 2-bit nibbles are replaced with the encoded X1' bit.

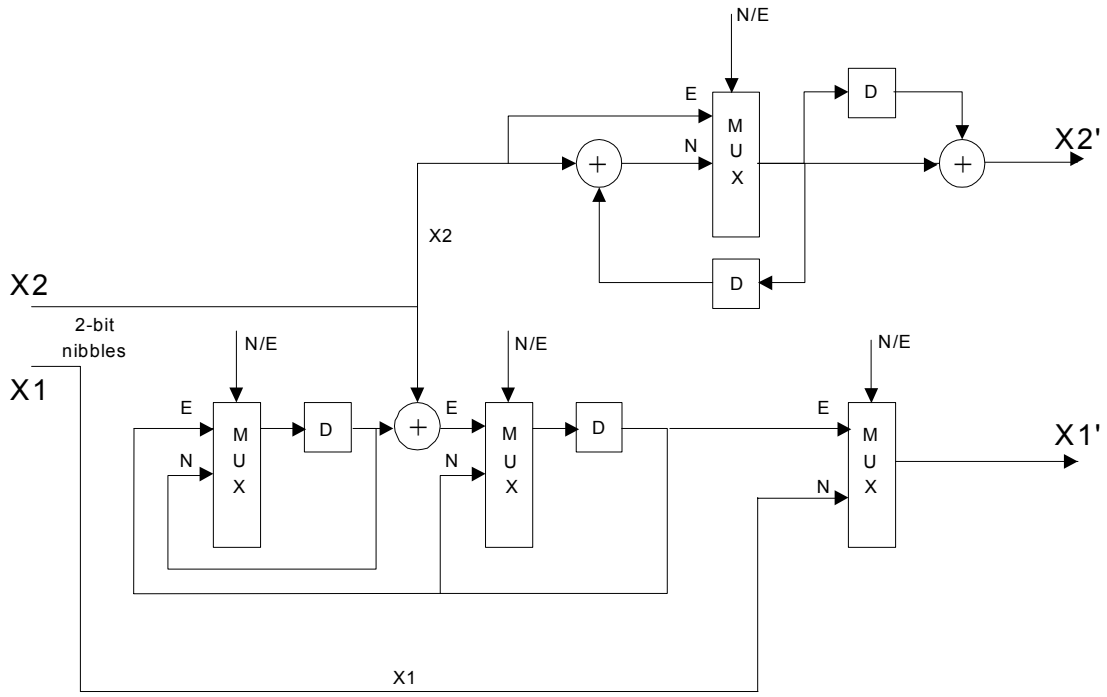


Figure D5.13 Enhanced Symbol Processor.

5.4.2.5.2 Precode bypass

The upper portion of Figure D5.13 illustrates the operation of the Precoder Bypass in the Enhanced symbol processor. The function of the Precoder Bypass is to produce a systematic trellis code for the Enhanced data (when the Enhanced convolutional encoder is concatenated with the normal trellis encoder), where Z2 is the information bit, Z1 is the output of the Enhanced convolutional encoder and derived from X1'.

For all robust transmission modes, the M/E flag selects the "E" input to the uppermost mux. The resulting X2' bit shown is then the derivative of the X2 bit. Upon subsequent Interference Filter Precoding, as depicted in Figure D5.8, the resulting Z2 bit produced is identical to the X2 bit in Figure D5.13. For the Main mode of transmission, the "M" input to the uppermost mux is selected, and the X2 bit is integrated and subsequently differentiated, therefore making the X2' bit identical to the X2 bit. Upon subsequent Interference Filter Precoding, the Y2 bit is achieved for the Main mode of transmission.

The normally encoded RS parity bytes of the Enhanced packets can introduce a phase inversion that produces an inverted systematic trellis code for the Enhanced data. Appropriate decoding of the Enhanced data depends on the Enhanced data trellis decoder's capability to decode either phase.

5.4.2.6 Data Byte De-Interleaver

The data byte de-interleaver is the inverse function of the Main convolutional interleaver.

5.4.2.7 RS Byte Delete and De-Randomizer

The RS parity bytes are removed and a de-randomizer, which is the inverse function of the Main randomizer, is applied to each byte of the 188-byte segment.

5.5 Synchronization

This section defines synchronization for data segments and fields.

5.5.1 Data Segment Sync

The encoded trellis data shall be passed through a multiplexer that inserts the various synchronization signals (Data Segment Sync and Data Field Sync).

A two-level (binary) 4-symbol Data Segment Sync shall be inserted into the 8-level digital data stream at the beginning of each Data Segment. (The MPEG-2 sync byte shall be replaced by Data Segment Sync.) The Data Segment Sync embedded in random data is illustrated in Figure D5.14.

A complete segment shall consist of 832 symbols: 4 symbols for Data Segment Sync, and 828 data plus parity symbols. The Data Segment Sync is binary (2-level). The same sync pattern occurs regularly at 77.3 μs intervals, and is the only signal repeating at this rate. Unlike the data, the four symbols for Data Segment Sync are not Reed-Solomon or trellis encoded, nor are they interleaved. The Data Segment Sync pattern shall be a 1001 pattern, as shown in Figure D5.14.

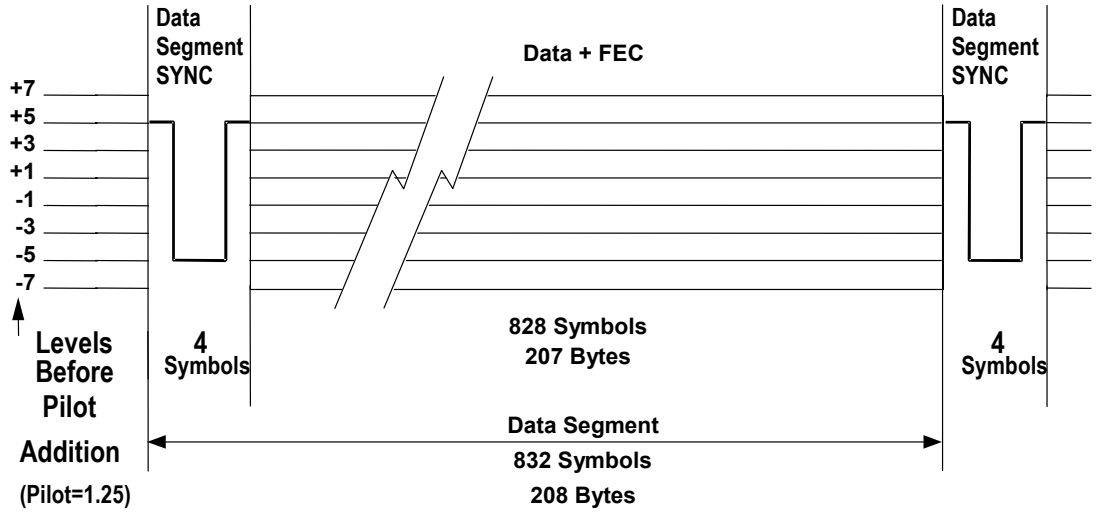


Figure D5.14 8-VSB data segment.

5.5.2 Data Field Sync

The data are not only divided into Data Segments, but also into Data Fields, each consisting of 313 segments. Each Data Field (24.2 ms) shall start with one complete Data Segment of Data Field Sync, as shown in Figure D5.15. Each symbol represents one bit of data (2-level). The arrangement of the 832 symbols in this segment are defined below. Refer to Figure D5.15 for the placement of these components during the data field sync. The sync in Figure D5.15 is the same as the Data Segment Sync and is defined as 1001.

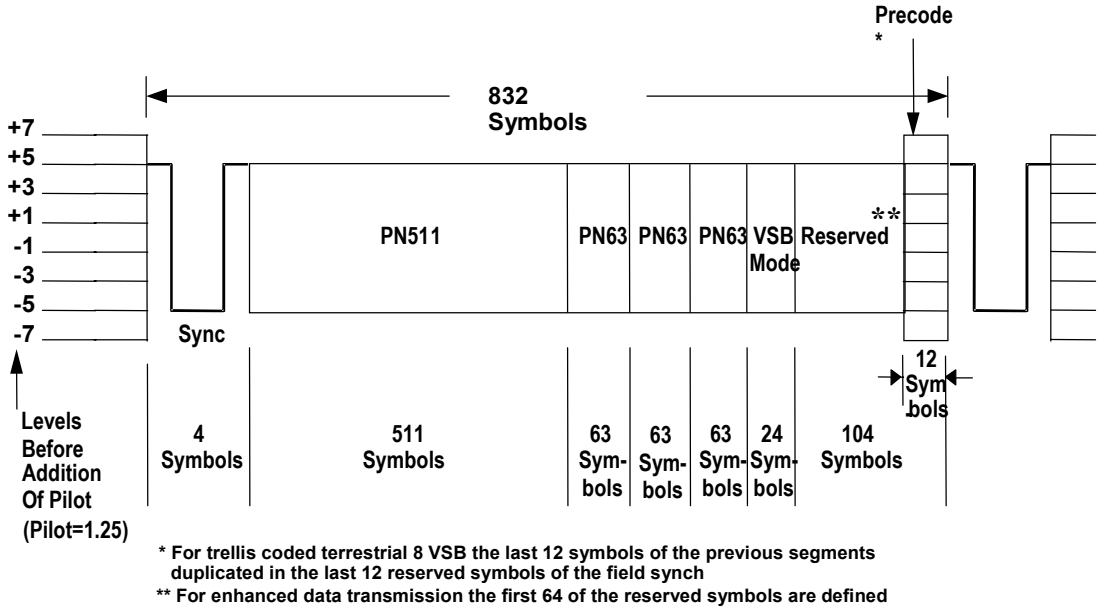


Figure D5.15 VSB data field sync.

5.5.2.1 Definition of the PN511 Sequence

This pseudo-random sequence is defined as $X^9 + X^7 + X^6 + X^4 + X^3 + X + 1$ with a pre-load value of 010000000. The sequence is:

0000 0001 0111 1111 1100 1010 1010 1110 0110 0110 1000 1000 1001 1110 0001 1101
0111 1101 0011 0101 0011 1011 0011 1010 0100 0101 1000 1111 0010 0001 0100 0111
1100 1111 0101 0001 0100 1100 0011 0001 0000 0100 0011 1111 0000 0101 0100 0000
1100 1111 1110 1110 1010 1001 0110 0110 0011 0111 0111 1011 0100 1010 0100 1110
0111 0001 0111 0100 0011 0100 1111 1011 0001 0101 1011 1100 1101 1010 1110 1101
1001 0110 1101 1100 1001 0010 1110 0011 1001 0111 1010 0011 0101 1000 0100 1101
1111 0001 0010 1011 1100 0110 0101 0000 1000 1100 0001 1110 1111 1101 0110 1010
1100 1001 1001 0001 1101 1100 0010 1101 0000 0110 1100 0000 1001 0000 0001 110

5.5.2.2 Definition of the PN63 Sequence

This pseudo-random sequence is repeated three times. It is defined as $X^6 + X + 1$ with a pre-load value of 100111. The middle PN63 is inverted on every other Data Field Sync. The sequence is:

1110 0100 1011 0111 0110 0110 1010 1111 1100 0001 0000 1100 0101 0011 1101 000

The generators for the PN63 and PN511 sequences are shown in Figure D5.16.

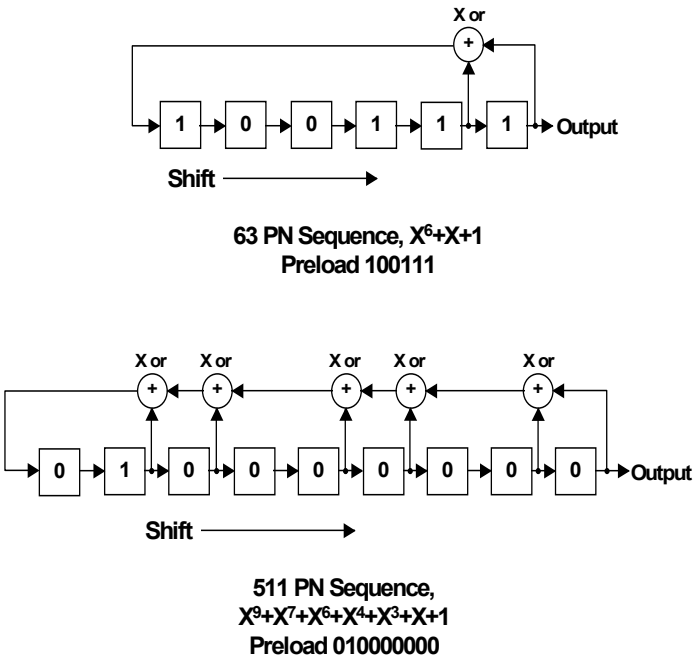


Figure D5.16 Field sync PN sequence generators.

5.5.2.3 VSB Mode Bits

These 24 bits determine the VSB mode for the data in the frame. The first two bytes are reserved. The fill pattern for these two bytes shall be '0000 1111 0000 1111' when 8 VSB is not signaled. The next byte is defined as:

P A B C $\overline{\text{P A B C}}$

where P is the even parity bit, the MSB of the byte, and A, B, C are the actual mode bits.

P	A	B	C	
0	0	0	0	Reserved
1	0	0	1	Reserved
1	0	1	0	Reserved
0	0	1	1	Reserved
1	1	0	0	16 VSB
0	1	0	1	8 VSB*
0	1	1	0	Reserved
1	1	1	1	Reserved

* In the 8 VSB mode, the preceding bits are defined as:

0 0 0 0 $\overline{\text{P A B C}}$ P A B C 1 1 1 1

5.5.2.4 Reserved

The last 104 bits shall be reserved space. It is suggested that this be filled with a continuation of the PN63 sequence. In the 8 VSB mode, 92 bits are reserved followed by the 12 symbol definition below.

5.5.2.5 Precode

In the 8 VSB mode, the last 12 symbols of the segment shall correspond to the last 12 symbols of the previous segment. All sequences are pre-loaded before the beginning of the Data Field Sync.

Like the Data Segment Sync, the Data Field Sync is not Reed-Solomon or trellis encoded, nor is it interleaved.

5.6 Enhanced Mode Data Rates

The Enhanced mix signaling in the data field sync provides 9 bits for selection of the mixture of Main, 1/2 rate and 1/4 rate data (512 choices). The tables for rate selection are formulated to provide denser packing at lower Enhanced data rates, to allow use of the minimum Enhanced data required by an application.

The amount of Main, 1/2 rate and 1/4 rate data present in a data frame shall be as indicated for that frame using one of the values from Table D5.3 which in turn references Tables D5.4*a*, and D5.4*b*.

Table D5.3, "Steps Numbers vs. Map Address," indicates an ordinal "Step Number" for each of the 1/2 rate and 1/4 rate data, corresponding to each 9-bit map address, with each bit labeled with a letter from "A" to "I". The three most significant bits (IHG) are shown in the top row and the six least significant bits (FEDCBA) of the map address are shown in the left column. The "Step Numbers" for the 1/2 rate data and 1/4 rate data corresponding to each 9-bit address are found at the intersection of the three-bit column address and the 6-bit row address.

Table D5.4*a*, "Rate Segments and Payload vs. Step Number – 1/2 Rate", indicates the number of data segments used by 1/2 rate data which shall be used for a given step number (which is referenced from Table D5.3).

Table D5.4*b*, "Rate Segments and Payload vs. Step Number – 1/4 Rate", indicates the number of data segments used by 1/4 rate data which shall be used for a given step number (which is referenced from Table D5.3).

Tables D5.4*a* and D5.4*b* also include informative columns. These columns show the approximate percent of segments allocated for Enhanced data, the payload of the Main data for the case when the Enhanced data consists of exclusively 1/2 rate or 1/4 rate data, and the payload of the Enhanced 1/4 or 1/2 rate data (respectively) for a given step number.

5.6.1 Enhanced Stream Rate Limits

Limits have been defined for the maximum bitrate in the Enhanced (E-VSB) service.

At all times, the quality of video in the main stream shall be equal to or better than the equivalent program in the Enhanced stream. In the event that the programming is different in the main and Enhanced streams, a higher resolution format is deemed to be higher quality.

Additionally, during premium programming times, the maximum bitrate in the enhanced (E-VSB) stream shall be 3 Mbps out of the total 19.4 Mbps channel capacity.

Of the map addresses 0_d to 511_d (notated as IHGFEDCBA in binary in Table D5.3) the decimal values of the only map addresses that shall be used when the 3 Mbps limit applies are: 0-70,72-77, 80-84, 88-90, 128-132, 136-139, 144-147, 152-154, 160-162, 168, 169, and 176.

Table D5.3 Steps vs. Map Address

IHG→ FEDCBA	000		001		010		011		100		101		110		111	
	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.
000000	0	0	0	8	8	0	8	8	0	17	17	0	0	25	0	29
000001	1	0	1	8	9	0	9	8	1	16	16	1	1	24	1	28
000010	2	0	2	8	10	0	10	8	2	17	17	2	2	25	3	29
000011	3	0	3	8	11	0	11	8	3	16	16	3	3	24	4	28
000100	4	0	4	8	12	0	12	8	4	17	17	4	4	25	6	29
000101	5	0	5	8	13	0	13	8	5	16	16	5	5	24	7	28
000110	6	0	6	8	14	0	14	8	6	17	17	6	6	25	9	29
000111	7	0	7	8	15	0	15	8	7	16	16	7	7	24	10	28
001000	0	1	0	9	8	1	8	9	8	17	17	8	8	25	12	28
001001	1	1	1	9	9	1	9	9	9	16	16	9	9	24	0	31
001010	2	1	2	9	10	1	10	9	10	17	17	10	10	25	2	30
001011	3	1	3	9	11	1	11	9	11	16	16	11	11	24	5	30
001100	4	1	4	9	12	1	12	9	12	17	17	12	12	25	16	17
001101	5	1	5	9	13	1	13	9	13	16	16	13	13	24	17	18
001110	6	1	6	9	14	1	14	9	14	17	17	14	14	25	16	19
001111	7	1	7	9	15	1	15	9	15	16	16	15	15	24	17	20
010000	0	2	0	10	8	2	8	10	0	19	19	0	0	27	16	21
010001	1	2	1	10	9	2	9	10	1	18	18	1	1	26	17	22
010010	2	2	2	10	10	2	10	10	2	19	19	2	2	27	16	23
010011	3	2	3	10	11	2	11	10	3	18	18	3	3	26	17	24
010100	4	2	4	10	12	2	12	10	4	19	19	4	4	27	16	25
010101	5	2	5	10	13	2	13	10	5	18	18	5	5	26	16	26
010110	6	2	6	10	14	2	14	10	6	19	19	6	6	27	18	19
010111	7	2	7	10	15	2	15	10	7	18	18	7	7	26	19	20
011000	0	3	0	11	8	3	8	11	8	19	19	8	8	27	18	21
011001	1	3	1	11	9	3	9	11	9	18	18	9	9	26	19	22
011010	2	3	2	11	10	3	10	11	10	19	19	10	10	27	18	23
011011	3	3	3	11	11	3	11	11	11	18	18	11	11	26	19	24
011100	4	3	4	11	12	3	12	11	12	19	19	12	12	27	18	25
011101	5	3	5	11	13	3	13	11	13	18	18	13	13	26	20	21
011110	6	3	6	11	14	3	14	11	14	19	19	14	14	27	21	22
011111	7	3	7	11	15	3	15	11	15	18	18	15	15	26	20	23
100000	0	4	0	12	8	4	8	12	0	21	21	0	25	0	29	0
100001	1	4	1	12	9	4	9	12	1	20	20	1	24	1	28	1
100010	2	4	2	12	10	4	10	12	2	21	21	2	25	2	29	3
100011	3	4	3	12	11	4	11	12	3	20	20	3	24	3	28	4
100100	4	4	4	12	12	4	12	12	4	21	21	4	25	4	29	6
100101	5	4	5	12	13	4	13	12	5	20	20	5	24	5	28	7
100110	6	4	6	12	14	4	14	12	6	21	21	6	25	6	29	9
100111	7	4	7	12	15	4	15	12	7	20	20	7	24	7	28	10
101000	0	5	0	13	8	5	8	13	8	21	21	8	25	8	28	12
101001	1	5	1	13	9	5	9	13	9	20	20	9	24	9	31	0
101010	2	5	2	13	10	5	10	13	10	21	21	10	25	10	30	2
101011	3	5	3	13	11	5	11	13	11	20	20	11	24	11	30	5
101100	4	5	4	13	12	5	12	13	12	21	21	12	25	12	17	16

IHG→ FEDCBA	000		001		010		011		100		101		110		111	
	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.	1/2 Step No.	1/4 Step No.
101101	5	5	5	13	13	5	13	13	13	20	20	13	24	13	18	17
101110	6	5	6	13	14	5	14	13	14	21	21	14	25	14	19	16
101111	7	5	7	13	15	5	15	13	15	20	20	15	24	15	20	17
110000	0	6	0	14	8	6	8	14	0	23	23	0	27	0	21	16
110001	1	6	1	14	9	6	9	14	1	22	22	1	26	1	22	17
110010	2	6	2	14	10	6	10	14	2	23	23	2	27	2	23	16
110011	3	6	3	14	11	6	11	14	3	22	22	3	26	3	24	17
110100	4	6	4	14	12	6	12	14	4	23	23	4	27	4	25	16
110101	5	6	5	14	13	6	13	14	5	22	22	5	26	5	26	16
110110	6	6	6	14	14	6	14	14	6	23	23	6	27	6	19	18
110111	7	6	7	14	15	6	15	14	7	22	22	7	26	7	20	19
111000	0	7	0	15	8	7	8	15	8	23	23	8	27	8	21	18
111001	1	7	1	15	9	7	9	15	9	22	22	9	26	9	22	19
111010	2	7	2	15	10	7	10	15	10	23	23	10	27	10	23	18
111011	3	7	3	15	11	7	11	15	11	22	22	11	26	11	24	19
111100	4	7	4	15	12	7	12	15	12	23	23	12	27	12	25	18
111101	5	7	5	15	13	7	13	15	13	22	22	13	26	13	21	20
111110	6	7	6	15	14	7	14	15	14	23	23	14	27	14	22	21
111111	7	7	7	15	15	7	15	15	15	22	22	15	26	15	23	20

Table D5.4*a* Segments and Payload vs. Step Number- 1/2 Rate

Step #	Segments Used	Percent of Segments Allocated for Enhanced (informative)	Main Data Rate (Mbps) (informative)	1/2 rate (Mbps) (informative)
0	0	0	19.3927	0.0000
1	2	0.64	19.2683	0.0542
2	4	1.28	19.144	0.1084
3	6	1.92	19.0197	0.1627
4	8	2.56	18.8954	0.2169
5	12	3.85	18.6468	0.3253
6	16	5.13	18.3982	0.4338
7	20	6.41	18.1495	0.5422
8	24	7.69	17.9009	0.6507
9	28	8.97	17.6523	0.7591
10	32	10.26	17.4037	0.8675
11	40	12.82	16.9064	1.0844
12	48	15.38	16.4092	1.3013
13	56	17.95	15.9119	1.5182
14	64	20.51	15.4147	1.7351
15	72	23.08	14.9174	1.9520
16	80	25.64	14.4202	2.1688
17	88	28.21	13.9229	2.3857
18	96	30.77	13.4257	2.6026
19	112	35.9	12.4312	3.0364
20	128	41.03	11.4367	3.4702
21	144	46.15	10.4422	3.9039
22	160	51.28	9.4477	4.3377
23	176	56.41	8.4532	4.7715
24	192	61.54	7.4587	5.2052
25	208	67.95	6.2156	5.6390
26	224	73.08	5.2211	6.0728
27	240	76.92	4.4752	6.5065
28	256	82.05	3.4807	6.9403
29	272	87.18	2.4862	7.3741
30	288	92.31	1.4917	7.8078
31	312	100	0	8.4585

Table D5.4*b* Segments and Payload vs. Step Number- 1/4 Rate

Step #	Segments Used	Percent of Segments Allocated for Enhanced (informative)	Main Data Rate (Mbps) (informative)	1/4 Rate (Mbps) (informative)
0	0	0.00	19.3927	0.0000
1	4	1.28	19.1440	0.0542
2	8	2.56	18.8954	0.1084
3	12	3.85	18.6468	0.1627
4	16	5.13	18.3982	0.2169
5	20	6.41	18.1495	0.2711
6	24	7.69	17.9009	0.3253
7	28	8.97	17.6523	0.3795
8	32	10.26	17.4037	0.4338
9	36	11.54	17.1550	0.4880
10	40	12.82	16.9064	0.5422
11	44	14.10	16.6578	0.5964
12	52	16.67	16.1605	0.7049
13	60	19.23	15.6633	0.8133
14	68	21.79	15.1661	0.9218
15	76	24.36	14.6688	1.0302
16	84	26.92	14.1716	1.1386
17	92	29.49	13.6743	1.2471
18	100	32.05	13.1771	1.3555
19	116	37.18	12.1826	1.5724
20	132	42.31	11.1881	1.7893
21	148	47.44	10.1936	2.0062
22	164	52.56	9.1991	2.2231
23	180	57.69	8.2046	2.4400
24	196	62.82	7.2101	2.6568
25	212	67.95	6.2156	2.8737
26	228	73.08	5.2211	3.0906
27	244	78.21	4.2266	3.3075
28	260	83.33	3.2321	3.5244
29	276	88.46	2.2376	3.7413
30	292	93.59	1.2431	3.9581
31	312	100.00	0.0000	4.2292

5.7 Enhanced Mode Map Bits

The signaling of the optional modes shall be done using the following bit assignments:

- The 64 two-level symbols in the data field sync immediately following the VSB mode bits shall be used to transmit the E8-VSB Enhanced segment locations during an Enhanced transmission.
- The map data shall indicate one of an allowed selection of possible Enhanced data mixes and segment arrangements, by means of an algorithm or look-up table. The data shall include a frame count indicating the next data frame at which the map will change.
- The map data shall be coded with a Kerdock (64, 12) code.
- The polarity of the Kerdock code word shall be inverted on even (negative PN63) data fields.

- The twelve-bit payload shall contain the current map or the next map.
- In the odd (positive PN63) field, the leftmost 10 bits shall indicate the current map and the rightmost 2 bits shall be the high order bits of the frame count.
- In the even (negative PN63) field the leftmost 10 bits shall indicate the next map and the rightmost 2 bits shall be the low order bits of the frame count.
- Within each frame count bit pair, the higher order bit shall be leftmost.

5.7.1 Map to Frame Count to Frame Association

The map shall change at a maximum frequency of once per 16 data frames.

A data frame shall be defined as an odd (positive PN63) data field followed by an even (negative PN63) data field.

The frame count shall be decremented linearly from 15 to 0 in the frames preceding a map change.

Current map data shall point one frame ahead, i.e., to the second frame following a particular transmission of the current map data.

Next map data shall point 16 frames ahead, i.e. to the 17^{th} frame following a particular transmission of the current map data.

An unchanging map shall be indicated by making the current map and next map equal and holding the frame count at 15 (1111).

An example of the sequence of map bits during a change is given in the Table D5.5. In this example, the map is changed from map A, which has persisted for some time, to map B, which then persists for some time into the future.

Table D5.5 Map Change Sequence

Frame Number	Frame Count	Map Data		Map Used
		Current Map	Next Map	
-3	15	A	A	A
-2	15	A	A	A
-1	15	A	B	A
0	15	A	B	A
1	14	A	B	A
2	13	A	B	A
3	12	A	B	A
4	11	A	B	A
5	10	A	B	A
6	9	A	B	A
7	8	A	B	A
8	7	A	B	A
9	6	A	B	A
10	5	A	B	A
11	4	A	B	A
12	3	A	B	A
13	2	A	B	A
14	1	A	B	A
15	0	B	B	A
16	15	B	B	B
17	15	B	B	B
18	15	B	B	B

5.7.2 Generation of Length of 64 Kerdock Codeword

The generator polynomial for the 64-bit Kerdock code word shall be

$$g(X) = \sum_{i=0}^{25} g_i X^i$$

where each g_i is an element of the row vector

$$g = \{1\ 1\ 1\ 2\ 0\ 1\ 2\ 2\ 0\ 1\ 0\ 3\ 0\ 3\ 1\ 3\ 3\ 0\ 1\ 3\ 2\ 1\ 2\ 2\ 1\ 3\}$$

with g_0 starting from the left.

The generator matrix shall be the following 6 x 32 matrix,

$$\text{gen\_matrix} = \begin{matrix} g_\alpha & g_0 & g_1 \ldots & g_{25} & 0 & 0 & 0 & 0 & 0 \\ g_\alpha & 0 & g_0 & g_1 \ldots & g_{25} & 0 & 0 & 0 & 0 \\ g_\alpha & 0 & 0 & g_0 & g_1 \ldots & g_{25} & 0 & 0 & 0 \\ g_\alpha & 0 & 0 & 0 & g_0 & g_1 \ldots & g_{25} & 0_0 & \\ g_\alpha & 0 & 0 & 0 & 0 & g_0 & g_1 \ldots & g_{25} & 0 \\ g_\alpha & 0 & 0 & 0 & 0 & 0 & g_0 & g_1 \ldots & g_{25} \end{matrix}$$

$$\text{where } g_\alpha = -\sum_{i=0}^{25} g_i \mod 4 = 1.$$

The resulting codeword shall be transmitted leftmost bit first.

5.7.3 Encoding Procedure

The 12 bit word to be encoded must first be transformed to the Z_4 domain word word_z4 by using the following mapping from bit pairs to modulo 4 digits.

$$0\ 0 \rightarrow 0$$
$$0\ 1 \rightarrow 1$$
$$1\ 1 \rightarrow 2$$
$$1\ 0 \rightarrow 3$$

After mapping to the Z_4 domain the word to be encoded is multiplied by the generator matrix.

$$\text{codeword\_z4} = [\text{word\_z4 x gen\_matrix}]$$

where word_z4 and codeword_z4 are row vectors.

Arithmetic operations are modulo 4.

The codeword is then converted back to binary using the following mapping.

$$0 \rightarrow 0\ 0$$
$$1 \rightarrow 0\ 1$$
$$2 \rightarrow 1\ 1$$
$$3 \rightarrow 1\ 0$$

Example:

Word to be encoded = 0 0 0 1 1 1 1 0 0 0 0 1.

Convert word to Z_4 domain.

$$\text{word\_z4} = 0\ 1\ 2\ 3\ 0\ 1$$

Multiply word_z4 by the generator matrix.

$$\text{codeword\_z4} = [\text{word\_z4 x gen\_matrix}]$$
$$= 301323001320002131023022301033 13$$

Convert codeword into binary.

codeword = 100001101110000001101100000011011001001110001111100001001010011 0

5.8 Enhanced Data Packing Structure

There are two options for distributing the Enhanced packets within the normal packets. Option 1 defines a distribution of the Enhanced packets, in packet number index, which are multiples of 4 segments. Option 2 defines a uniform distribution of the Enhanced packets within the normal packet frame. Option 1 optimizes carrier to noise ratio performance. Option 2 optimizes performance in the presence of dynamic multipath.

The 10^{th} bit of the 12-bit E-VSB map shall decide which packing structure is to be used in the VSB frame. When the bit is set to 0, the packing shall refer to and be per packing option 1 defined below. When the bit is set to 1, the packing shall refer to and be per packing option 2 defined below.

5.8.1 Placement of Enhanced Mode Packets

Let 2P be the total number of Enhanced packets transmitted in a VSB frame, where 0<=P<= 156. Let the index s of the Enhanced packets inserted in the normal VSB frame be an interger between 0 and 311, Inclusive.

Option 1

The set *EMAP* of E8-VSB segment positions *s* shall be:

For 0<= P <= 39
EMAP = {s | s = 4i, i = 0,1,…,2P-1}, (0 <= s <= 311)

For 40<= P <= 78
EMAP = {s | s = 4i, i = 0,1,…,77} U {s | s = 4i+2, i = 0,1,…,2P-79}

For 79<= P <= 117
EMAP = {s | s = 4i, i = 0,1,…,77}
U {s | s = 4i+2, i = 0,1,…,77}
U {s | s = 4i+1, i = 0,1,…,2P-157}

For 118<= P <= 156 :
EMAP = {s | s = 4i, i = 0,1,…,77}
U {s | s = 4i+2, i = 0,1,…,77}
U {s | s = 4i+1, i = 0,1,…,77}
U {s | s = 4i+3, i = 0,1,…,2P-235}

Where U is the union of sets, and {s | s =…criteria…} is the set of segment positions s that meet the stated criteria.

Option 2

The index s shall be calculated by the following algorithm written in pseudo-code.

```
M=round(156/P);

for k=0:2P-1
    s=k*M;
    if (s>312)
        s=mod(s, 312)+1;
    end if
end for
```

The function round() means "round up to the next integer value." The function mod() represents the operation modulo. For example, in case of P=6, the segment positions are given by s=(0, 26, 52, 78, 104, 130,156 , 182, 208, 234, 260, 286).

5.8.2 Packing of Enhanced Mode Data Within Packets

The Enhanced Reed-Solomon encoding block shall be 184 bytes long, of which 20 bytes are parity. Refer to Table D5. 2.

For the case of a 1/2 rate Enhanced code, the Enhanced coder outputs 2 bits for each input bit, and Enhanced mode data shall be packed as one Enhanced Reed-Solomon block to a pair of data segments (1 bit per symbol).

For the case of a 1/4 rate Enhanced code, the Enhanced coder outputs 4 bits for each input bit, and Enhanced mode data shall be packed as one Enhanced Reed-Solomon block for every 4 data segments (1/2 bit per symbol).

The packing of Enhanced mode Reed-Solomon blocks into data segments is shown in Table D5.6.

> Note: All below are shown conceptually pre-interleave; the interleaving process will disperse the data in the transmitted output).

Table D5.6 Enhanced Data Encapsulation

For 1/2 Rate Outer Code			
tx hdr (12 symbols) 3 bytes	E8-VSB data (736 symbols) Payload 92 bytes		Main RS parity (80 symbols) 20 Bytes
tx hdr (12 symbols) 3 bytes	E8-VSB data (576 symbols) Payload 72 bytes	E8-VSB RS parity (160 symbols) 20 bytes	Main RS parity (80 symbols) 20 bytes
tx hdr (12 symbols) 3 bytes	E8-VSB data (736 symbols) Payload 92 bytes		Main RS parity (80 symbols) 20 bytes
tx hdr (12 symbols) 3 bytes	E8-VSB data (576 symbols) Payload 72 bytes	E8-VSB RS parity (160 symbols) 20 bytes	Main RS parity (80 symbols) 20 bytes
2 bits/symbol	1 bit/symbol		2 bits/symbol
For 1/4 Rate Outer Code			
tx hdr (12 symbols) 3 bytes	E8-VSB data (736 symbols) Payload 46 bytes		Main RS parity (80 symbols) 20 bytes
tx hdr (12 symbols) 3 bytes	E8-VSB data (736 symbols) Payload 46 bytes		Main RS parity (80 symbols) 20 bytes
tx hdr (12 symbols) 3 bytes	E8-VSB data (736 symbols) Payload 46 bytes		Main RS parity (80 symbols) 20 bytes
tx hdr (12 symbols) 3 bytes	E8-VSB data (416 symbols) Payload 26 bytes	E8-VSB RS parity (320 symbols) 20 bytes	Main RS parity (80 symbols) 20 bytes
2 bits/symbol	0.5 bit/symbol		2 bits/symbol

5.9 Modulation

5.9.1 Bit-to-Symbol Mapping

Figure D5.8 shows the mapping of the outputs of the trellis decoder to the nominal signal levels of (–7, –5, –3, –1, 1, 3, 5, 7). As shown in Figure D5.14, the nominal levels of Data Segment Sync and Data Field Sync are –5 and +5. The value of 1.25 is added to all these nominal levels after the bit-to-symbol mapping function for the purpose of creating a small pilot carrier.

5.9.2 Pilot Addition

A small in-phase pilot shall be added to the data signal. The frequency of the pilot shall be the same as the suppressed-carrier frequency as shown in Figure D5.4. This may be generated in the

following manner. A small (digital) DC level (1.25) shall be added to every symbol (data and sync) of the digital baseband data plus sync signal (±l, ±3, ±5, ±7). The power of the pilot shall be 11.3 dB below the average data signal power.

5.9.3 8 VSB Modulation Method

The VSB modulator receives the 10.76 Msymbols/s, 8-level trellis encoded composite data signal (pilot and sync added). The ATV system performance is based on a linear phase raised cosine Nyquist filter response in the concatenated transmitter and receiver, as shown in Figure D5.17. The system filter response is essentially flat across the entire band, except for the transition regions at each end of the band. Nominally, the roll-off in the transmitter shall have the response of a linear phase root raised cosine filter.

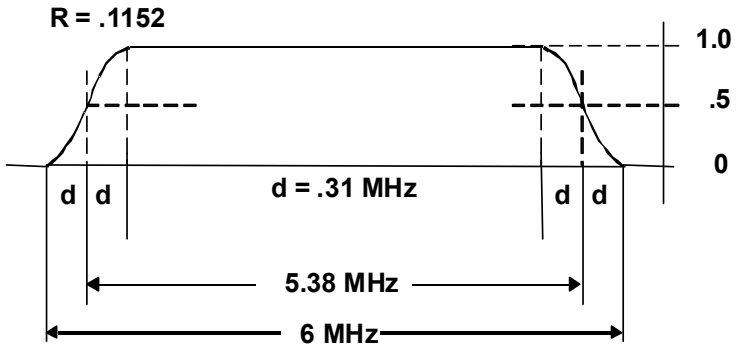


Figure D5.17 Nominal VSB system channel response (linear phase raised cosine Nyquist filter).

6. TRANSMISSION CHARACTERISTICS FOR HIGH DATA RATE MODE

6.1 Overview

The high data rate mode trades off transmission robustness (28.3 dB signal-to-noise threshold) for payload data rate (38.57 Mbps). Most parts of the high data rate mode VSB system are identical or similar to the terrestrial system. A pilot, Data Segment Sync, and Data Field Sync are all used to provide enhanced operation. The pilot in the high data rate mode also is 11.3 dB below the data signal power. The symbol, segment, and field signals and rates are all the same, allowing either receiver to lock up on the other's transmitted signal. Also, the data frame definitions are identical. The primary difference is the number of transmitted levels (8 versus 16) and the use of trellis coding and NTSC interference rejection filtering in the terrestrial system.

The RF spectrum of the high data rate modem transmitter looks identical to the terrestrial system, as illustrated in Figure D5.4. Figure D6.1 illustrates a typical data segment, where the number of data levels is seen to be 16 due to the doubled data rate. Each portion of 828 data symbols represents 187 data bytes and 20 Reed-Solomon bytes followed by a second group of 187 data bytes and 20 Reed-Solomon bytes (before convolutional interleaving).

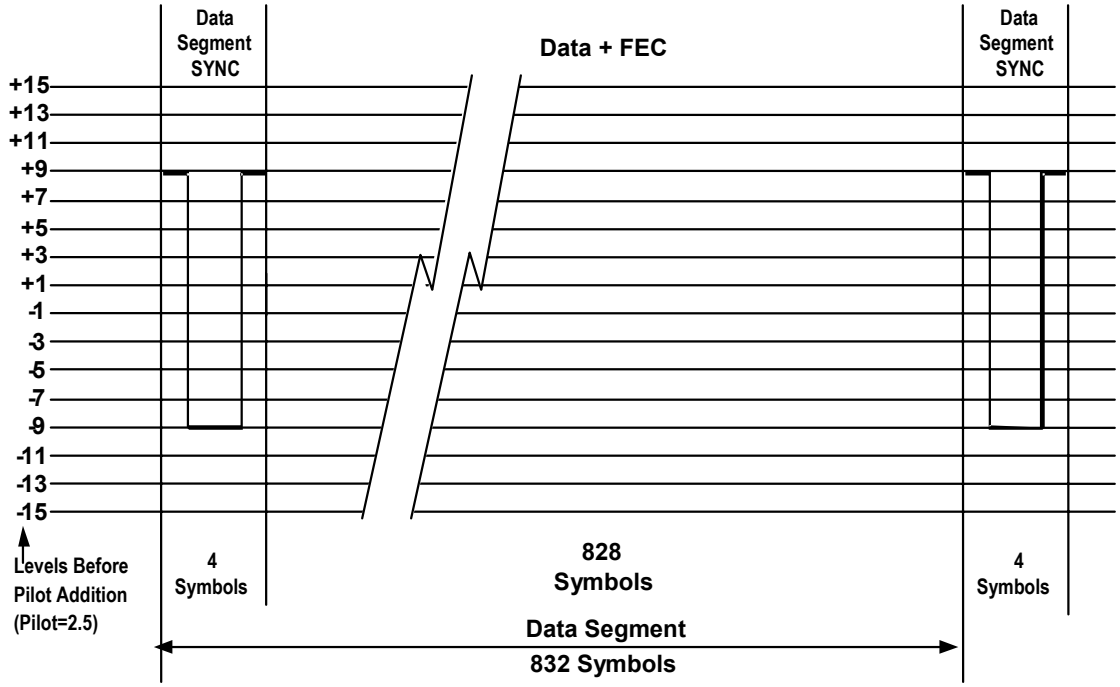


Figure D6.1 16-VSB data segment.

Figure D6.2 shows the block diagram of the transmitter. It is identical to the terrestrial VSB system except the trellis coding shall be replaced with a mapper that converts data to multi-level symbols. See Figure D6.3.

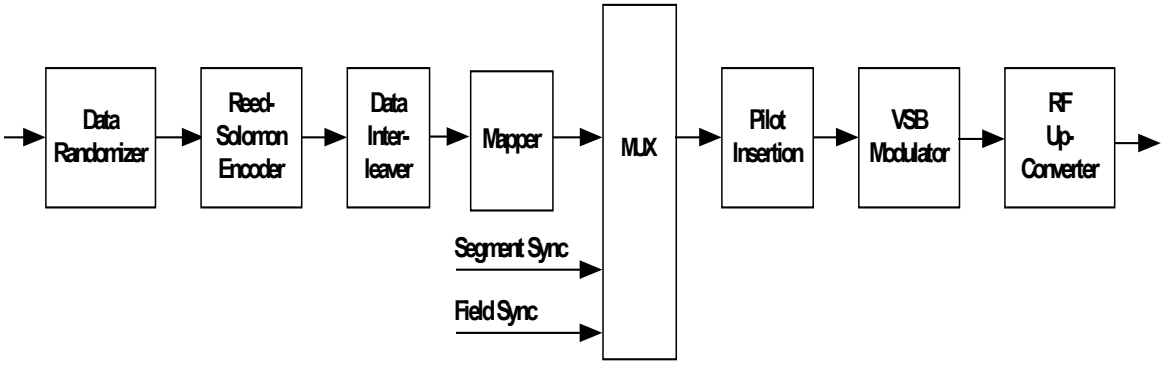


Figure D6.2 16 VSB transmitter.

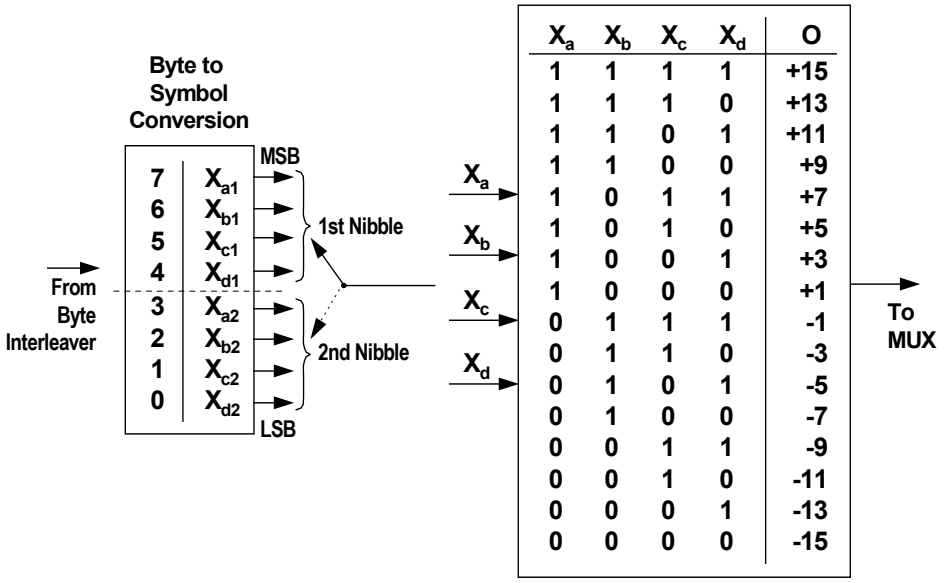


Figure D6.3 16 VSB mapper.

6.2 Channel Error Protection and Synchronization

6.2.1 Data Randomizer

See Section 5.4.1.1.

6.2.2 Reed-Solomon Encoder

See Section 5.4.1.2.

6.2.3 Interleaving

The interleaver shall be a 26 data segment inter-segment convolutional byte interleaver. Interleaving is provided to a depth of about 1/12 of a data field (2 ms deep). Only data bytes shall be interleaved.

6.2.4 Data Segment Sync

See Section 5.5.1.

6.2.5 Data Field Sync

See Section 5.5.2.

6.3 Modulation

6.3.1 Bit-to-Symbol Mapping

Figure D6.3 shows the mapping of the outputs of the interleaver to the nominal signal levels (–15, –13, –11, ..., 11, 13, 15). As shown in Figure D6.1, the nominal levels of Data Segment Sync and Data Field Sync are –9 and +9. The value of 2.5 is added to all these nominal levels after the bit-to-symbol mapping for the purpose of creating a small pilot carrier.

6.3.2 Pilot Addition

A small in-phase pilot shall be added to the data signal. The frequency of the pilot shall be the same as the suppressed-carrier frequency as shown in Figure D5.4. This may be generated in the following manner. A small (digital) DC level (2.5) shall be added to every symbol (data and sync) of the digital baseband data plus sync signal ($\pm$l, $\pm$3, $\pm$5, $\pm$7, $\pm$9, $\pm$11, $\pm$13, $\pm$15). The power of the pilot shall be 11.3 dB below the average data signal power.

6.3.3 16 VSB Modulation Method

The modulation method shall be identical to that in Section 5.9.3, except the number of transmitted levels shall be 16 instead of 8.